Recommended schedule

Day 1

Topics: *Logic states and simple gate circuits*
Questions: *1 through 10*
Lab Exercise: *OR gate, diode-resistor logic (question 51)*

Day 2

Topics: *TTL logic gates and truth tables*
Questions: *11 through 20*
Lab Exercise: *AND gate, simple BJT logic (question 52)*

Day 3

Topics: *CMOS logic gates and truth tables*
Questions: *21 through 30*
Lab Exercise: *IC logic gate usage (question 53)*

Day 4

Topics: *Relay circuits and truth tables*
Questions: *31 through 40*
Lab Exercise: *AND gate, relay logic (question 54)*

Day 5

Topics: *Logic circuit performance parameters*
Questions: *41 through 50*
Lab Exercise: *Gate-relay interposing (question 55)*

Day 6

Exam 1: *includes IC logic gate performance assessment*

Troubleshooting practice problems

Questions: *57 through 66*

DC/AC review problems

Questions: *67 through 86*

Basic principles of microcontrollers

Questions: *87 through 96*

General concept practice and challenge problems

Questions: *97 through the end of the worksheet*

Impending deadlines

Project due at end of ELTR140, Section 3
Question 56: Sample project grading criteria

Project ideas

Logic probe: Uses a comparator and at least one logic gate to drive three LEDs: "High", "Low", and "Indeterminate", showing three different voltage levels detected at the probe. The thresholds for high and low logic levels shall be adjustable for use in different types of logic circuits.

Digital combination lock: Drives a solenoid or other power device only when the input code matches the "key" code (set by a series of switches on the circuit board), and drives an alarm siren if the input code does *not* match the "key" code. The logic function may be done with Exclusive-OR gates or with a magnitude comparator IC. Remember, the more bits in the codes, the harder it is to guess!

Skill standards addressed by this course section

EIA *Raising the Standard; Electronics Technician Skills for Today and Tomorrow*, June 1994

F Technical Skills – Digital Circuits

F.01 Demonstrate an understanding of the characteristics of integrated circuit (IC) logic families.
F.05 Understand principles and operations of types of logic gates.
F.06 Fabricate and demonstrate types of logic gates.
F.07 Troubleshoot and repair types of logic gates.

B Basic and Practical Skills – Communicating on the Job

B.01 Use effective written and other communication skills. *Met by group discussion and completion of labwork.*
B.03 Employ appropriate skills for gathering and retaining information. *Met by research and preparation prior to group discussion.*
B.04 Interpret written, graphic, and oral instructions. *Met by completion of labwork.*
B.06 Use language appropriate to the situation. *Met by group discussion and in explaining completed labwork.*
B.07 Participate in meetings in a positive and constructive manner. *Met by group discussion.*
B.08 Use job-related terminology. *Met by group discussion and in explaining completed labwork.*
B.10 Document work projects, procedures, tests, and equipment failures. *Met by project construction and/or troubleshooting assessments.*

C Basic and Practical Skills – Solving Problems and Critical Thinking

C.01 Identify the problem. *Met by research and preparation prior to group discussion.*
C.03 Identify available solutions and their impact including evaluating credibility of information, and locating information. *Met by research and preparation prior to group discussion.*
C.07 Organize personal workloads. *Met by daily labwork, preparatory research, and project management.*
C.08 Participate in brainstorming sessions to generate new ideas and solve problems. *Met by group discussion.*

D Basic and Practical Skills – Reading

D.01 Read and apply various sources of technical information (e.g. manufacturer literature, codes, and regulations). *Met by research and preparation prior to group discussion.*

E Basic and Practical Skills – Proficiency in Mathematics

E.01 Determine if a solution is reasonable.
E.02 Demonstrate ability to use a simple electronic calculator.
E.06 Translate written and/or verbal statements into mathematical expressions.
E.07 Compare, compute, and solve problems involving binary, octal, decimal, and hexadecimal numbering systems.
E.12 Interpret and use tables, charts, maps, and/or graphs.
E.13 Identify patterns, note trends, and/or draw conclusions from tables, charts, maps, and/or graphs.
E.15 Simplify and solve algebraic expressions and formulas.
E.16 Select and use formulas appropriately.
E.18 Use properties of exponents and logarithms.

F Additional Skills – Electromechanics

B.01b Relays and relay circuits.

Common areas of confusion for students

Difficult concept: *Necessary conditions for transistor operation.*

It is vitally important for students to understand the conditions necessary for transistor operation, both for understanding how circuits work and for troubleshooting faulty circuits. Bipolar junction transistors require a base current (in the proper direction) to conduct, and the collector-to-emitter voltage must be of the correct polarity to push a collector current in the proper direction as well. Both currents join at the emitter terminal, making the emitter current the sum of the base and collector currents. Field-effect transistors are not so picky about the direction of the controlled current, and they only require the correct gate voltage (no gate current) to establish conduction. What makes this so confusing is that there are two types of bipolar transistors (NPN and PNP), two types of junction field-effect transistors (N-channel and P-channel), and four types of MOSFETs (E-type N-channel, E-type P-channel, D-type N-channel, and D-type P-channel).

Difficult concept: *Current sourcing versus current sinking.*

It is very common in electronics work to refer to current-controlling devices as either *sourcing* current to a load or *sinking* current from a load. This is an overt reference to conventional-flow notation, referring to whether the conventional flow moves *out* of the transistor from the positive power supply terminal to the load (sourcing), or whether the conventional flow moves *in* to the transistor from the load and then "down" to ground (sinking). Some students grasp this concept readily, while others seem to struggle mightily with it. It is something rather essential to understand, because this terminology is extensively used by electronics professionals and found in electronics literature. The key detail distinguishing the two conditions is which power supply rail (either +V or Gnd) is *directly* connected to the current-controlling device.

Difficult concept: *Pullup and pulldown resistor placement.*

In digital circuits, resistors are often used to provide a secure logic state when an input device (such as a switch) goes to a high-impedance (open) mode. Students often have difficulty figuring out exactly where these resistors should go in a circuit. The most common mistake I've seen is to place one of these "pullup" or "pulldown" resistors in *series* with a gate input, which will accomplish absolutely nothing. The "trick" to getting this placement right, if you can call it a trick at all, is to literally follow the word "pullup" or "pulldown." A *pullup* resistor pulls the logic state of a wire up to the positive supply rail, and so must connect between the gate input and +V. A *pulldown* resistor pulls the logic state of a wire down to ground potential, and so must connect between the gate input and ground. In either case, the resistor provides a sure path to the opposite power rail that the input device connects to when active (closed).

Question 1

A rheostat (variable resistor) and a switch are both examples of electric components exhibiting different degrees of conductivity:

Which of these devices would be considered *discrete* and which would be considered *continuous* in terms of their electrical conductivity? What do each of these words mean, and how might they apply to variables in electric circuits other than conductivity?

file 02753

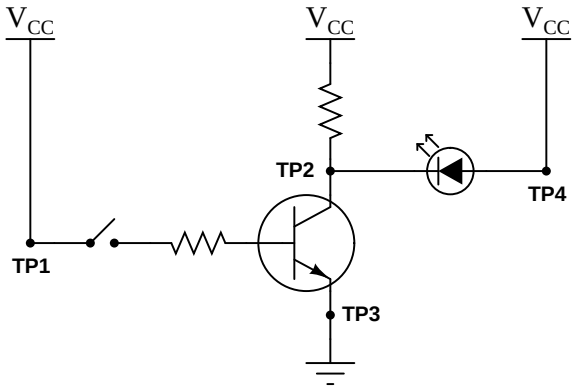
Question 2

Digital logic circuitry makes use of discrete voltage levels: each "logic gate" sub-circuit inputs and outputs voltages that are either considered "high" or "low". Define what both of these terms means in a digital logic circuit powered by 5 volts DC.

file 02755

Question 3

Determine the logic levels (either "high" or "low") at each of the test points in this circuit with the toggle switch in the open position, as well as the status of the transistor and LED:

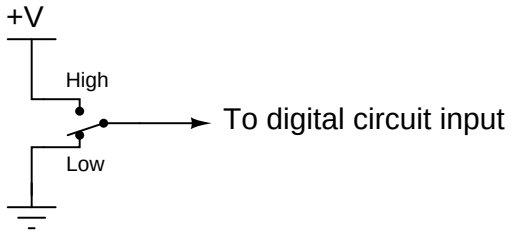


- V_{TP1} = (*high* or *low*?)
- V_{TP2} = (*high* or *low*?)
- V_{TP3} = (*high* or *low*?)
- V_{TP4} = (*high* or *low*?)
- Transistor = (*on* or *off*?)
- LED = (*on* or *off*?)

file 02756

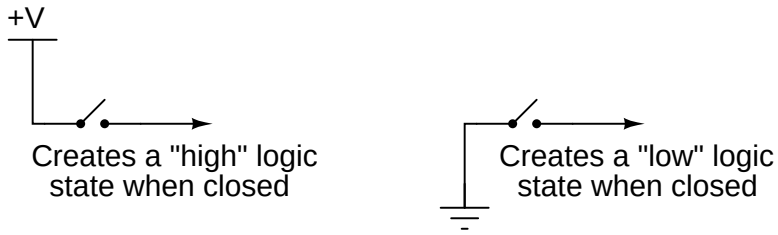
Question 4

If we need to produce a discrete logic signal ("high" or "low") from a mechanical switch, the most direct way of doing so is to use a single-pole, double-throw switch (SPDT) like this:

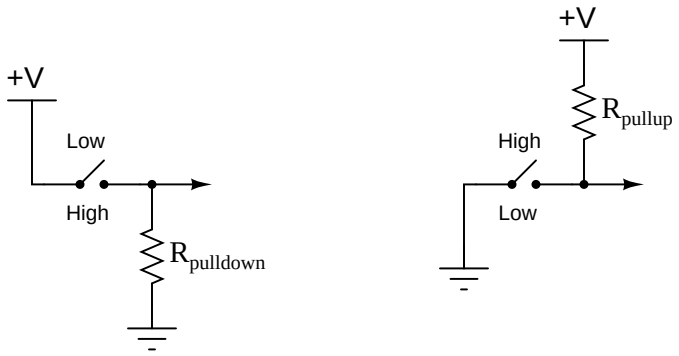


In the "High" position, the switch directly connects the signal line to +V, ensuring a high logic state; in the "Low" position, the switch directly connects the signal line to ground, ensuring a low logic state. What could be simpler?

However, often a SPDT switch is not feasible and we must use a SPST (single-pole, single-throw) switch instead:



A problem often arises with such configurations because in the open position there is neither a connection to +V nor ground. In other words, these two SPST configurations produce the exact same indeterminate logic state ("floating") when their respective switches are open. To remedy this, resistors are often added to such circuits:

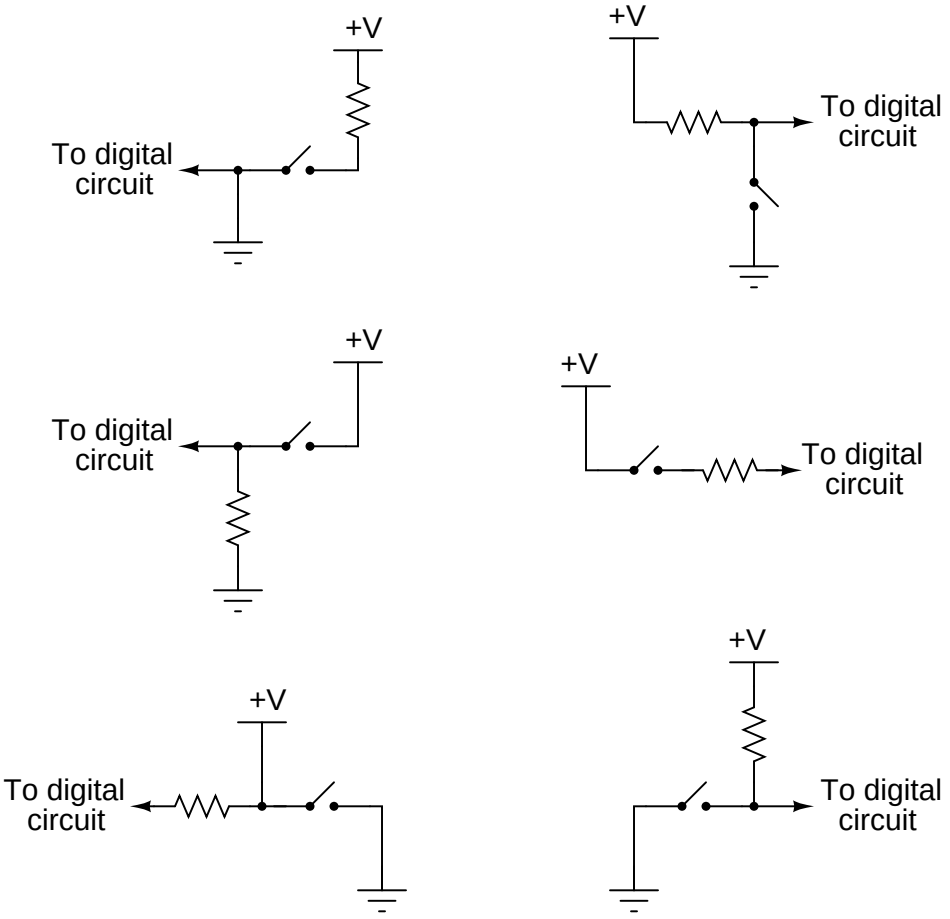


Explain what functions the *pulldown* and *pullup* resistors serve, and also why they are referred to by those names.

file 03001

Question 5

A common mistake made by students new to digital circuits is to misplace the pullup or pulldown resistors in schematic diagrams, and also in the circuits they build. Study the following schematics and determine whether the resistor in each one is a properly-placed *pullup* or *pulldown* resistor, or if it is improperly placed:

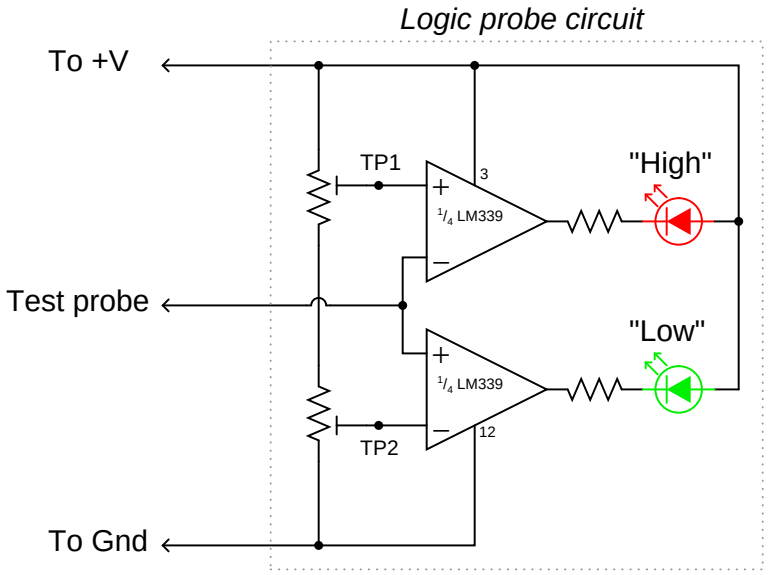


file 03181

Question 6

A *logic probe* is a very useful tool for working with digital logic circuits. It indicates "high" and "low" logic states by means of LED's, giving visual indication only if the voltage levels are appropriate for each state.

Here is a schematic diagram for a logic probe built using comparators. Each comparator has a threshold adjustment potentiometer, so that it may be set to indicate its respective logic state only if the signal voltage is well within the range stated by the logic manufacturer:

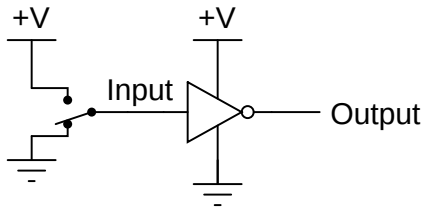


Explain how this circuit functions.

file 02758

Question 7

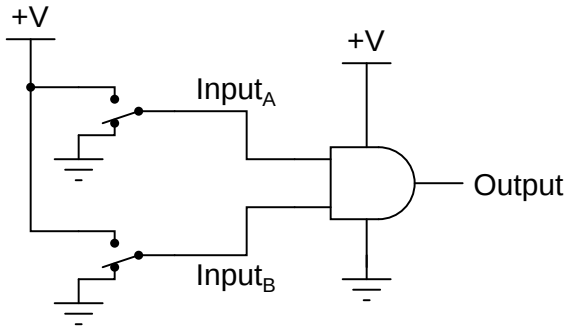
Identify the type of logic gate shown in this schematic diagram, and explain why it has the name it does:



file 02761

Question 8

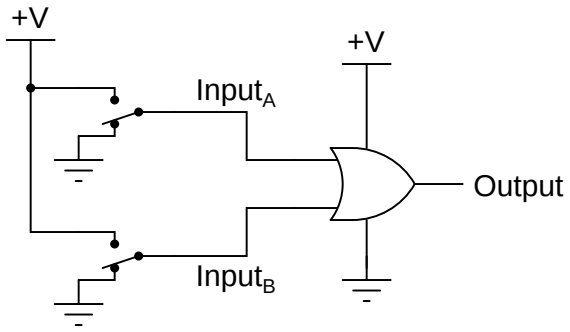
Identify the type of logic gate shown in this schematic diagram, and explain why it has the name it does:



file 02760

Question 9

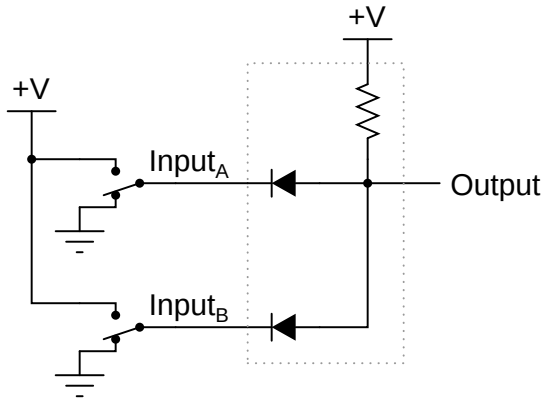
Identify the type of logic gate shown in this schematic diagram, and explain why it has the name it does:



file 02759

Question 10

Crude logic gates circuits may be constructed out of nothing but diodes and resistors. Take for example this logic gate circuit:

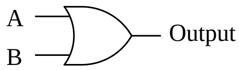


Identify what type of logic function is represented by this gate circuit (AND, OR, inverter, etc.). Also, trace the directions of all currents in this circuit.

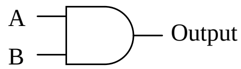
file 02762

Question 11

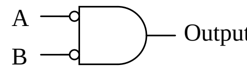
Identify each of these logic gates by name, and complete their respective truth tables:



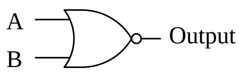
A	B	Output
0	0	
0	1	
1	0	
1	1	



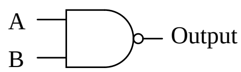
A	B	Output
0	0	
0	1	
1	0	
1	1	



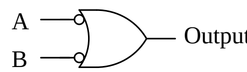
A	B	Output
0	0	
0	1	
1	0	
1	1	



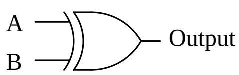
A	B	Output
0	0	
0	1	
1	0	
1	1	



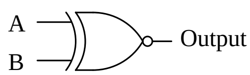
A	B	Output
0	0	
0	1	
1	0	
1	1	



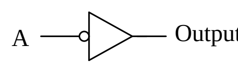
A	B	Output
0	0	
0	1	
1	0	
1	1	



A	B	Output
0	0	
0	1	
1	0	
1	1	



A	B	Output
0	0	
0	1	
1	0	
1	1	

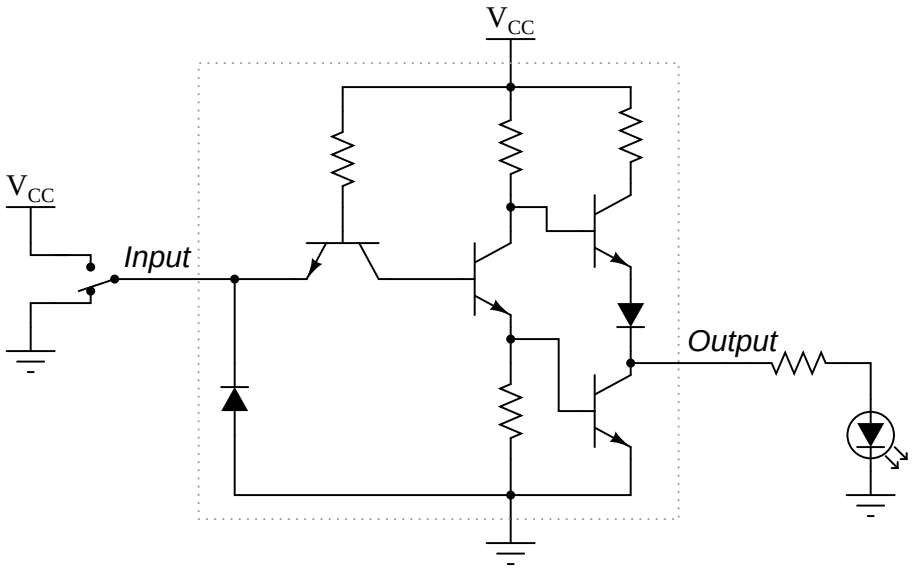


A	Output
0	
1	

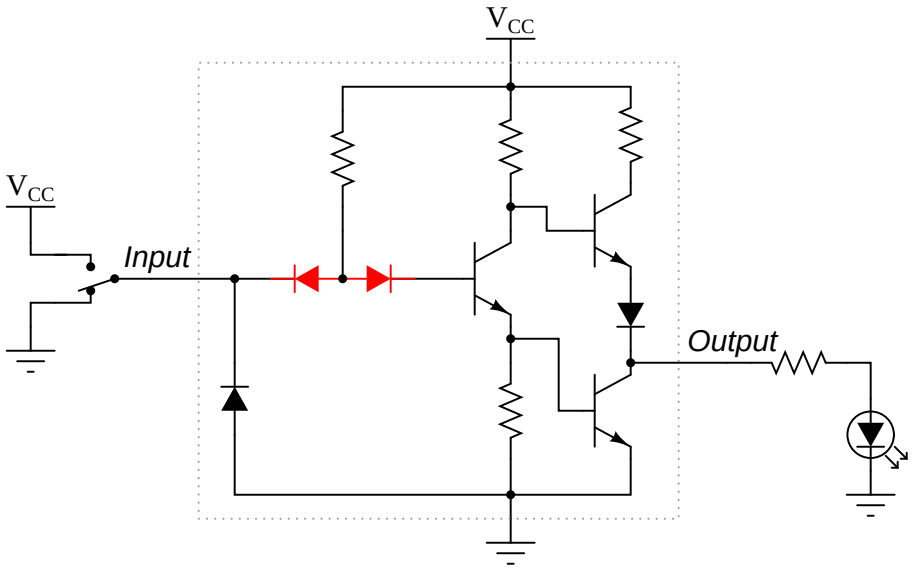
file 01249

Question 12

The simplest type of digital logic circuit is an *inverter*, also called an *inverting buffer*, or *NOT gate*. Here is a schematic diagram for an inverter gate constructed from bipolar transistors (transistor-to-transistor-logic, also known as *TTL*), shown connected to a SPDT switch and an LED:



The left-most transistor in this schematic is actually not being used as a transistor, but rather it functions as a "steering diode" network, like this:



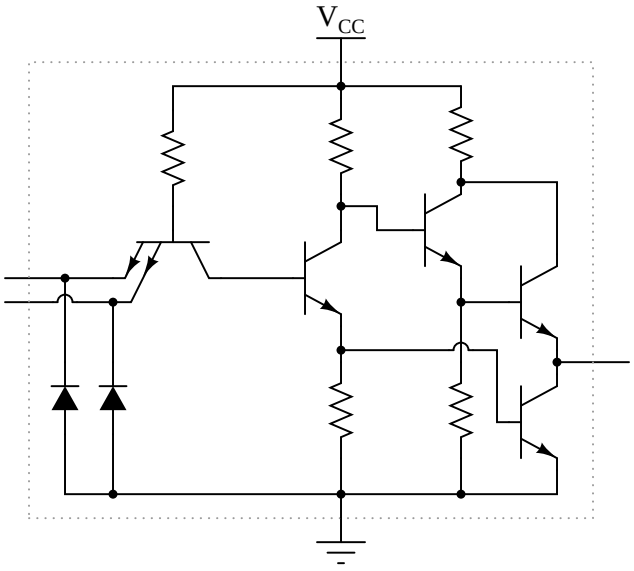
Determine the status of the LED in each of the input switch's two positions. Denote the logic level of switch and LED in the form of a truth table:

Input	Output

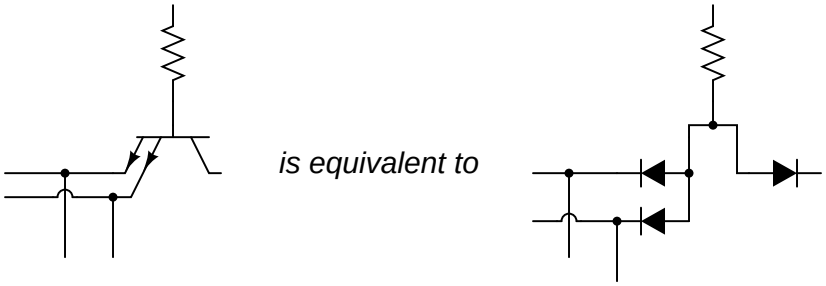
file 01256

Question 13

The following is an internal schematic of a TTL logic gate. Based on your analysis of the transistor circuit, determine what type of gate (AND, OR, NAND, NOR, XOR, etc.) it is:



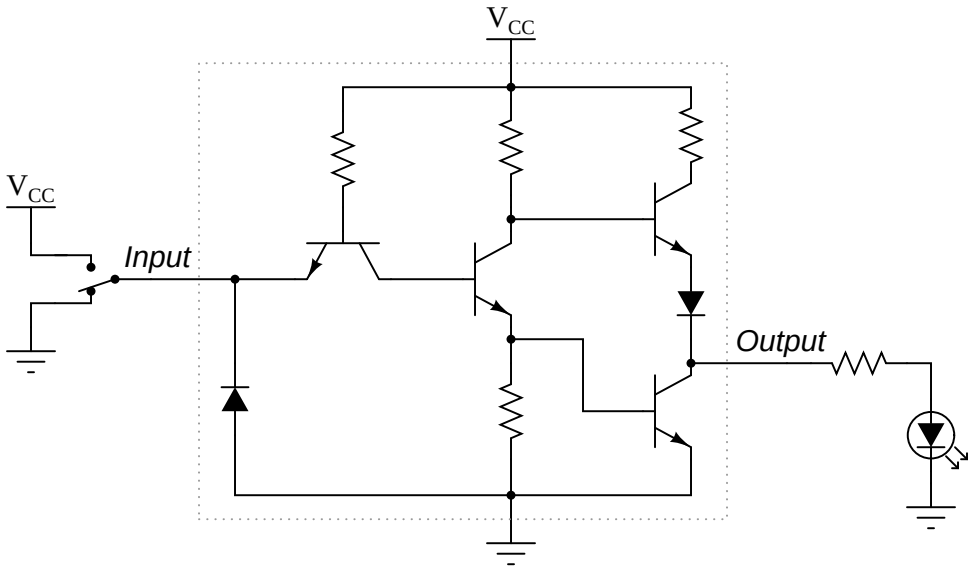
Hint: the double-emitter transistor is being used as a pair of diodes, and not as an amplifying device!



file 01250

Question 14

A very important concept to understand in digital circuitry is the difference between *current sourcing* and *current sinking*. For instance, examine this TTL inverter gate circuit, connected to a load:

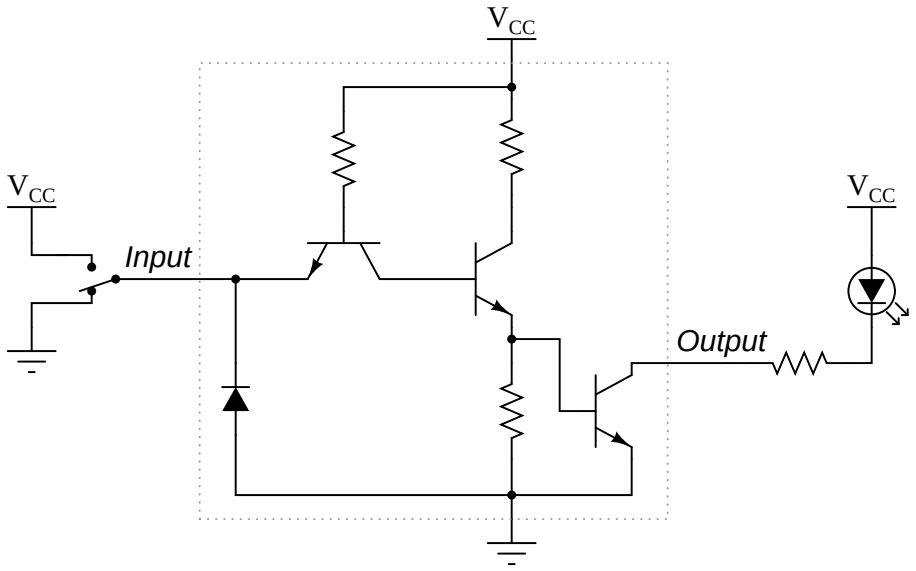


The output circuitry of this particular gate is commonly referred to as "totem-pole," because the two output transistors are stacked one above the other like figures on a totem pole. Is a gate circuit with a totem-pole output stage able to *source* load current, *sink* load current, or do both?

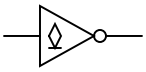
file 01666

Question 15

A very important concept to understand in digital circuitry is the difference between *current sourcing* and *current sinking*. For instance, examine this open-collector TTL inverter gate circuit, connected to a load:



Open-collector gates are specially designated in their schematic symbols by a marker within the gate shape:



Is this gate circuit able to *source* load current, *sink* load current, or do both?

file 01258

Question 16

Based on an analysis of a typical TTL logic gate circuit (consult a datasheet for a TTL logic gate if you need an internal schematic diagram for a gate circuit), determine what logic state is "assumed" by a TTL gate input when left "floating" (disconnected).

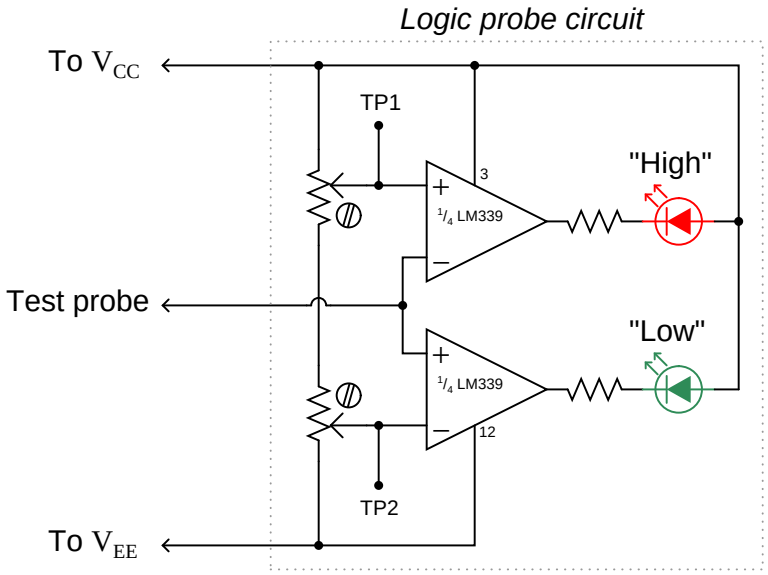
What ramification does this have for us when choosing input devices for TTL logic gates? If, for instance, we wished to use a single-pole, single-throw (SPST) switch as the input device for a TTL logic gate, what is the *best* way to connect such a device to a TTL input? Should the switch connect the TTL input to V_{CC} when closed, or should it connect the input to V_{EE} when closed? Why does it matter? Explain your answer in detail.

file 01257

Question 17

A *logic probe* is a very useful tool for working with digital logic circuits. It indicates "high" and "low" logic states by means of LED's, giving visual indication only if the voltage levels are appropriate for each state.

Here is a schematic diagram for a logic probe built using comparators. Each comparator has a threshold adjustment potentiometer, so that it may be set to indicate its respective logic state only if the signal voltage is well within the range stated by the logic manufacturer:

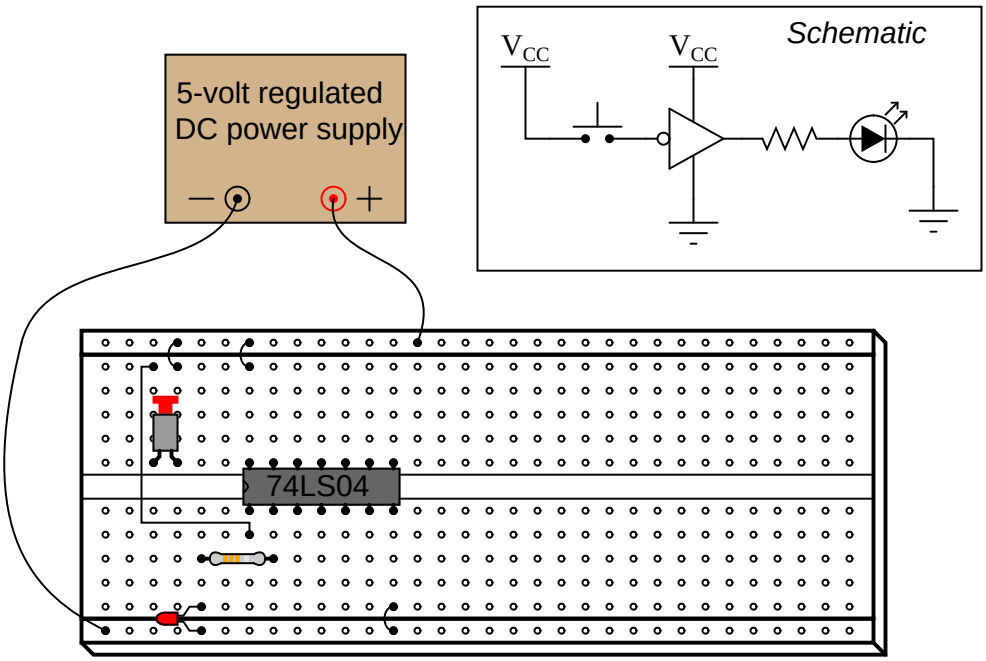


When this logic probe circuit is connected to the V_{CC} and V_{EE} power supply terminals of a powered TTL circuit, what voltage levels should test points TP1 and TP2 be adjusted to, in order for the probe to properly indicate "high" and "low" TTL logic states? Consult a datasheet for the quad NAND gate numbered either 74LS00 or 54LS00. Both are legacy TTL integrated circuits.

file 01262

Question 18

A student builds the following digital circuit on a solderless breadboard (a "proto-board"):



The DIP circuit is a TTL hex inverter (it contains *six* "inverter" or "NOT" logic gates), but only one of these gates is being used in this circuit. The student's intent was to build a logic circuit that energized the LED when the pushbutton switch was unactuated, and de-energized the LED when the switch was pressed: so that the LED indicated the reverse state of the switch itself. However, in reality the LED fails to energize no matter what state the switch is in.

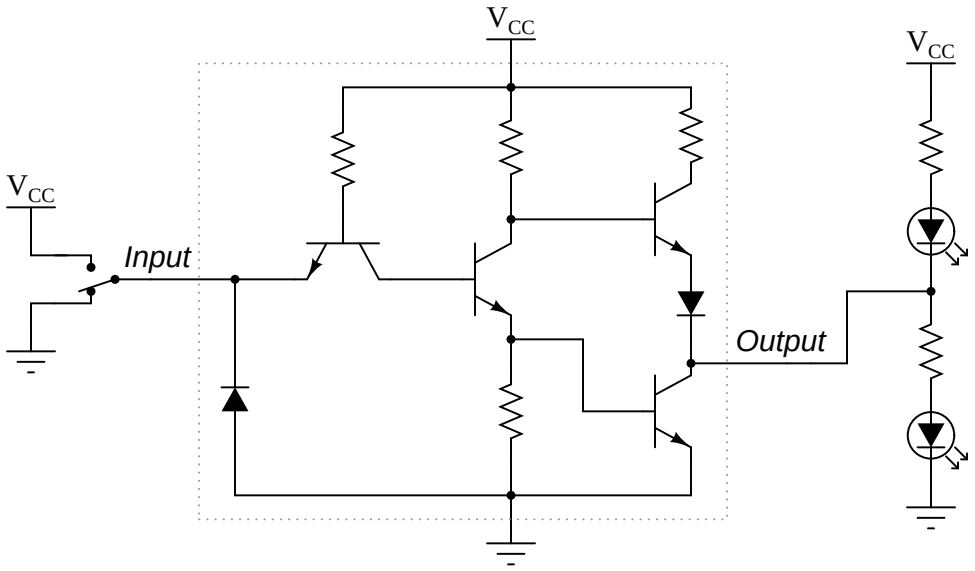
First question: how would you use a multimeter as a logic probe to check the logic states of points in this circuit, in order to troubleshoot it?

Second question: suppose you checked the logic states of pin #1 on the IC, for both states of the switch (pressed and unpressed), and found that pin #1 was always "high". How does this measurement indicate the student's design flaw in this circuit? How would you recommend this design flaw be corrected?

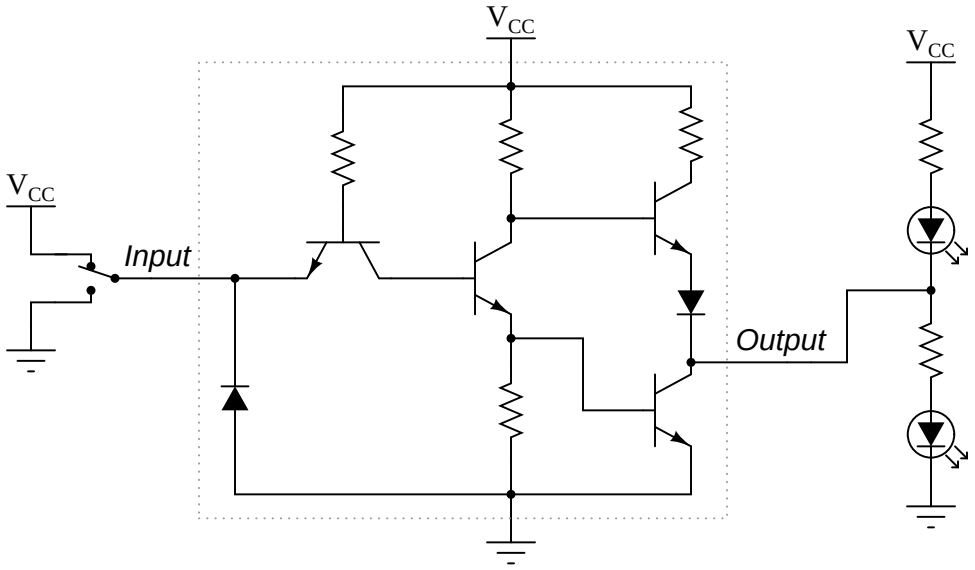
file 01252

Question 19

Draw the paths of all currents in this circuit with the input in a "low" state:



Now, draw the paths of all currents in this circuit with the input in a "high" state:



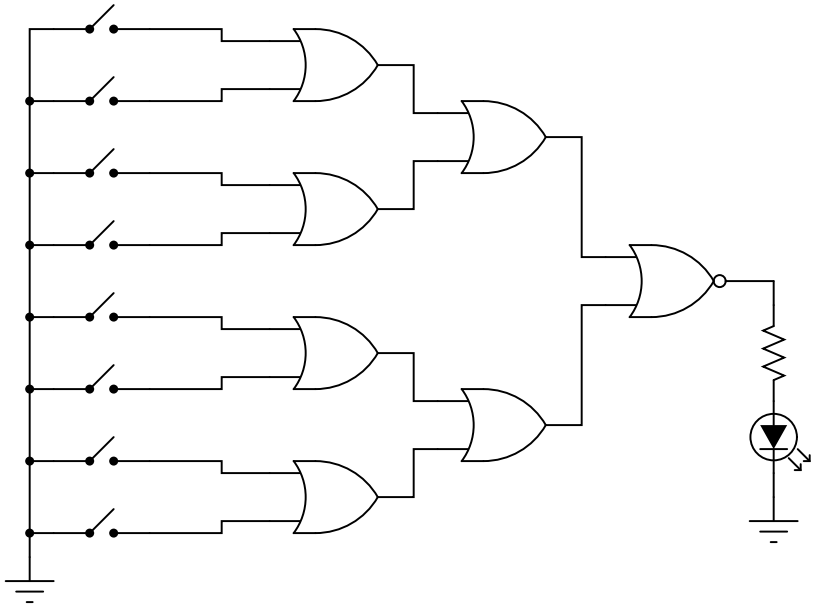
Where is the power supplied for each LED? What relationship is there between the load current (LED) and the gate input current (through the SPDT switch)?

Also, explain how you would calculate the values for appropriate LED current-limiting resistors in this circuit.

file 02904

Question 20

The digital circuit shown here is a unanimous-yea vote detector. Votes are cast by eight different voters by the setting of switches in either the closed (yea) or open (nay) positions. According to the logic function provided by the TTL gates, the LED will energize if and only if all switches are closed:



As is common in digital circuit schematics, the power supply (V_{CC}) is omitted for the sake of simplicity. This is analogous to the omission of power supply connections in many operational amplifier circuit schematics.

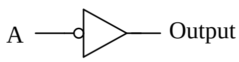
If we were to draw a truth table for this circuit, how large (number of rows and columns) would the table have to be?

Suppose we wished to modify this circuit, such that an electromechanical bell would ring whenever a unanimous-yea vote was cast, rather than merely lighting a small LED. The bell we have in mind to use is rather large, its solenoid coil drawing 3 amps of current at a voltage of 12 volts DC: well beyond the final gate's ability to source. How could we modify this circuit so that the final gate is able to energize this bell instead of just an LED?

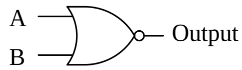
file 01260

Question 21

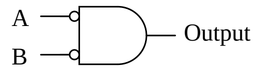
Identify each of these logic gates by name, and complete their respective truth tables:



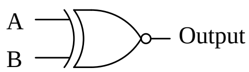
A	Output
0	
1	



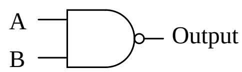
A	B	Output
0	0	
0	1	
1	0	
1	1	



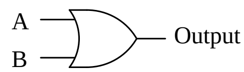
A	B	Output
0	0	
0	1	
1	0	
1	1	



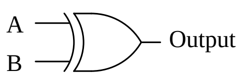
A	B	Output
0	0	
0	1	
1	0	
1	1	



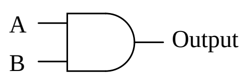
A	B	Output
0	0	
0	1	
1	0	
1	1	



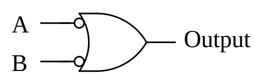
A	B	Output
0	0	
0	1	
1	0	
1	1	



A	B	Output
0	0	
0	1	
1	0	
1	1	



A	B	Output
0	0	
0	1	
1	0	
1	1	

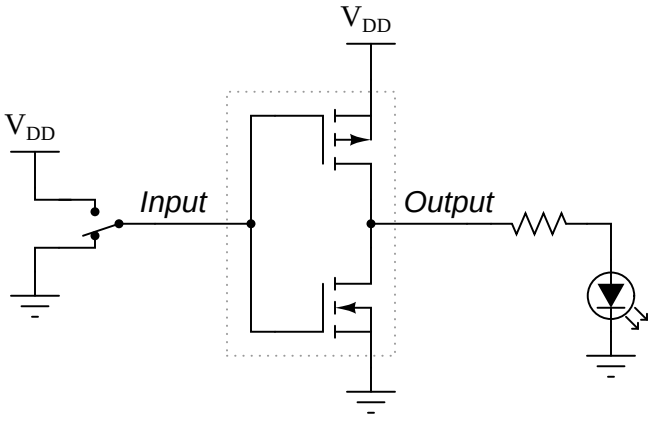


A	B	Output
0	0	
0	1	
1	0	
1	1	

file 02772

Question 22

The simplest type of digital logic circuit is an *inverter*, also called an *inverting buffer*, or *NOT gate*. Here is a schematic diagram for an inverter gate constructed from complementary MOSFETs (CMOS), shown connected to a SPDT switch and an LED:



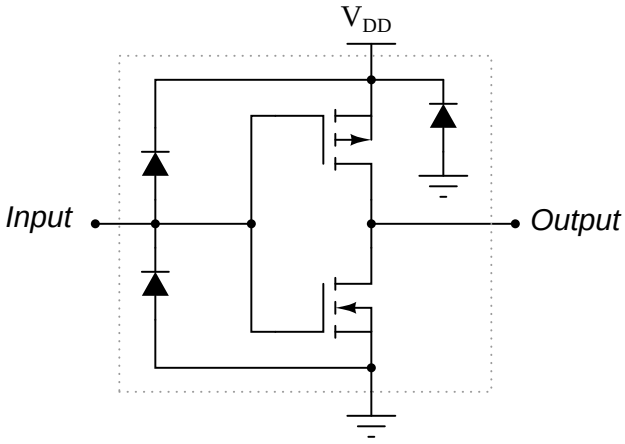
Determine the status of the LED in each of the input switch's two positions. Denote the logic level of switch and LED in the form of a truth table:

Input	Output

file 01254

Question 23

Practical CMOS logic gates contain more than just MOSFETs. Here is a schematic diagram for a typical inverter gate circuit, with protection diodes:

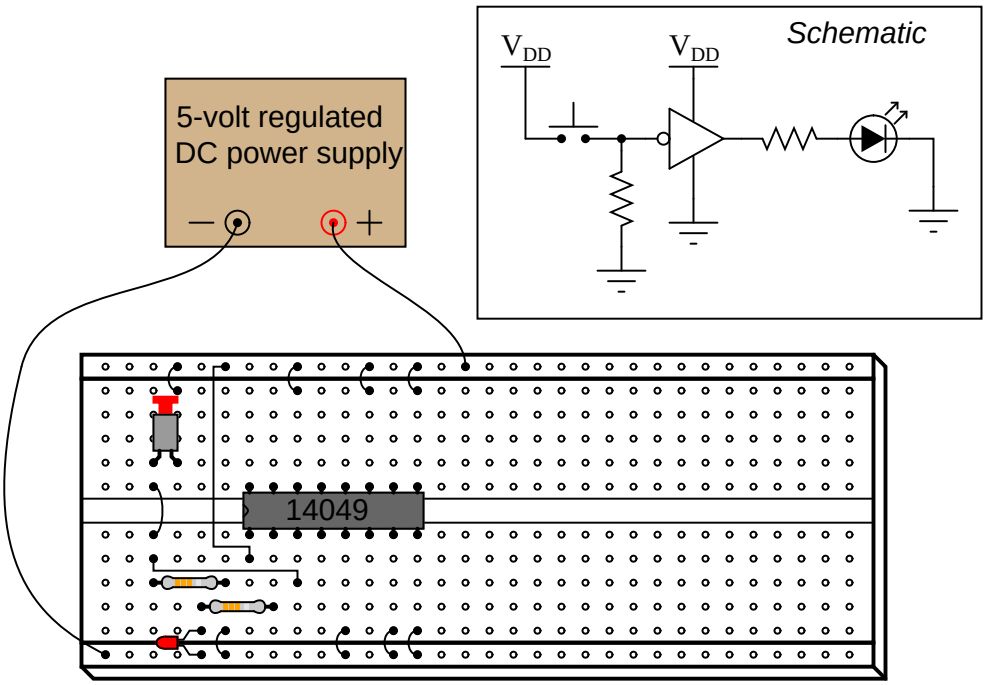


Explain what specific conditions each protection diode protects against.

file 01255

Question 24

A student builds the following digital circuit on a solderless breadboard (a "proto-board"):



The DIP circuit is a hex inverter (it contains *six* "inverter" or "NOT" logic gates), but only one of these gates is being used in this circuit. The student's intent was to build a logic circuit that energized the LED when the pushbutton switch was unactuated, and de-energized the LED when the switch was pressed: so that the LED indicates the reverse state of the switch itself. The student builds this circuit, and it is found to function perfectly well.

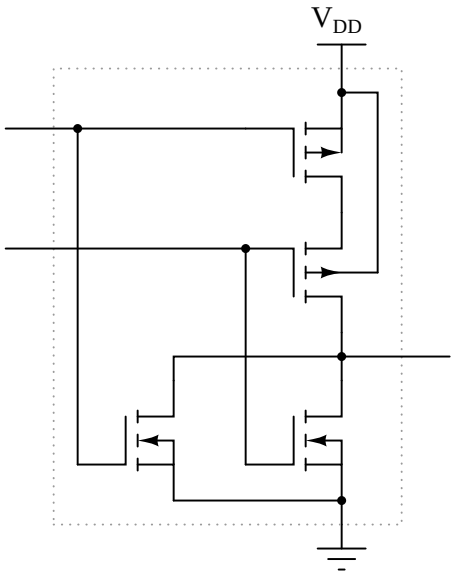
Explain the purpose of the resistor on the input of the inverter. What is it there for? What might happen if it were to be removed from the circuit?

Also, explain why the inputs of all the unused inverter gates in this IC have been either connected to ground or to V_{DD}. Is this necessary for the circuit to work properly, or is it just a precautionary measure?

file 01253

Question 25

The following is an internal schematic of a CMOS logic gate. Based on your analysis of the transistor circuit, determine what type of gate (AND, OR, NAND, NOR, XOR, etc.) it is:



file 01272

Question 26

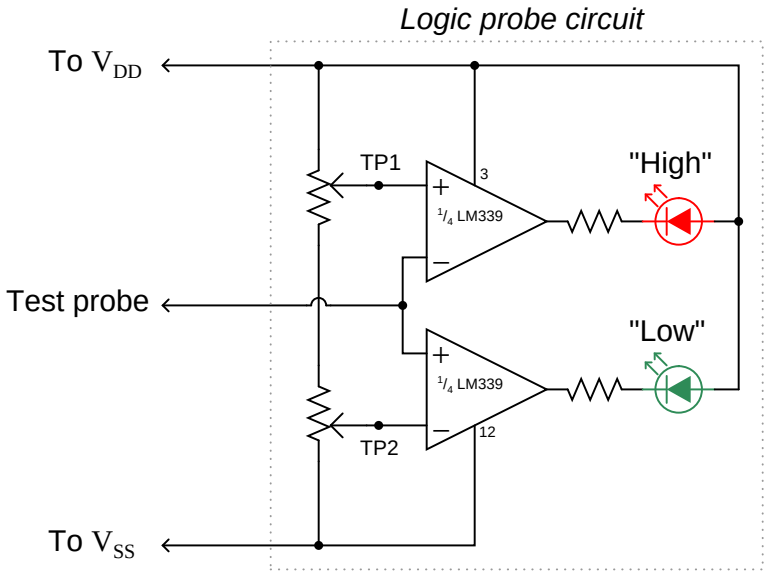
What is the typical power supply voltage range for a CD4xxx series (or MC4xxx series) CMOS logic gate? How does this compare with the allowable power supply voltage range for a standard (5 volt) TTL logic gate? Consult a datasheet for your answer.

file 01274

Question 27

A *logic probe* is a very useful tool for working with digital logic circuits. It indicates "high" and "low" logic states by means of LED's, giving visual indication only if the voltage levels are appropriate for each state.

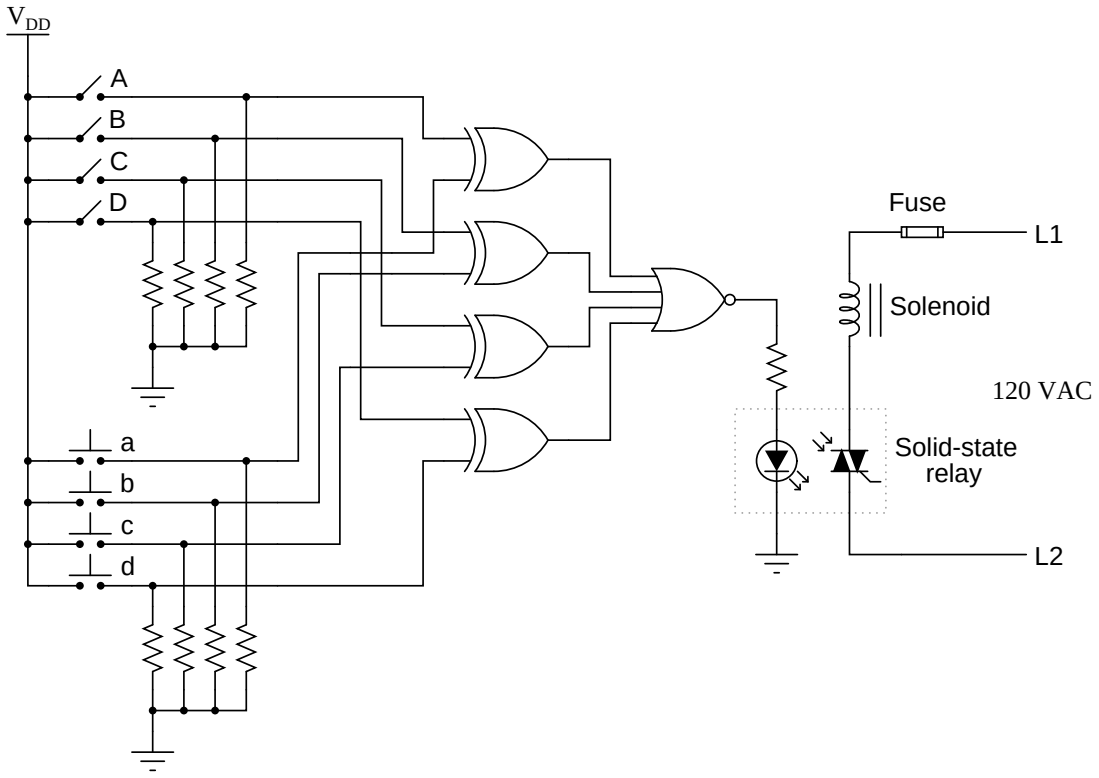
Here is a schematic diagram for a logic probe built using comparators. Each comparator has a threshold adjustment potentiometer, so that it may be set to indicate its respective logic state only if the signal voltage is well within the range stated by the logic manufacturer:



When this logic probe circuit is connected to the V_{DD} and V_{SS} power supply terminals of a powered CMOS circuit, what voltage levels should test points TP1 and TP2 be adjusted to, in order for the probe to properly indicate "high" and "low" CMOS logic states? Consult a datasheet for the quad NAND gate numbered 4011. This is a legacy CMOS integrated circuit. file 01275

Question 28

Here is a schematic diagram for a simple electronic combination lock, controlling power to a door lock solenoid:



The four pushbutton switches (a, b, c, and d) are accessible to the person wishing to enter the door. The four toggle switches (A, B, C, and D) are located behind the door, and are used to set the code necessary for entering.

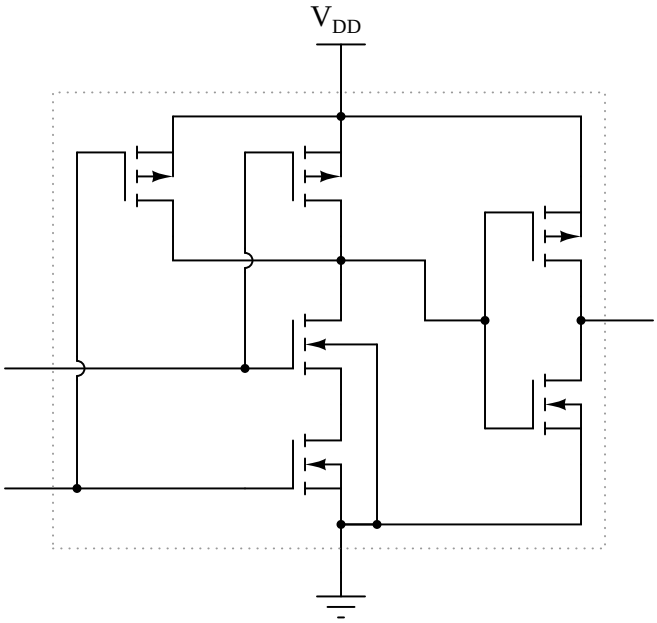
Explain how this system is supposed to work. What are the logic states of the respective gate outputs when a matching code is entered through the pushbutton switches? How about when a non-matching code is entered?

Do you see any security problems with this door lock circuit? How easy would it be for someone to enter, who does not know the four-bit code? Do you have any suggestions for improving this lock design?

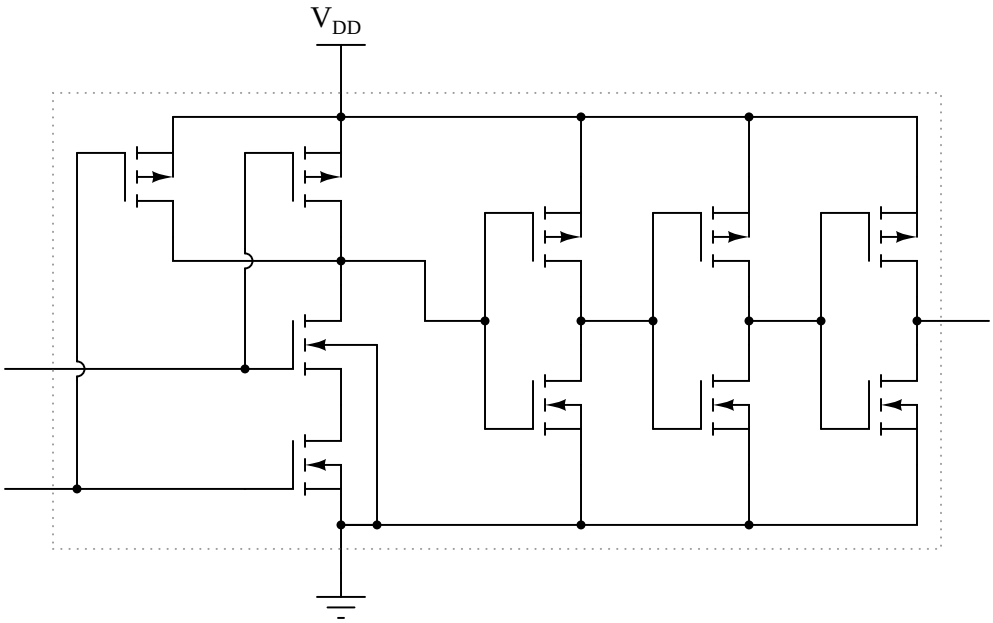
file 01277

Question 29

Many modern CMOS gate circuits are *buffered* with additional transistor stages on their outputs. For example, an unbuffered AND gate is shown here, with no more transistors than is necessary to fulfill the "AND" logic function:



One type of "buffered" CMOS AND gate looks like this:



As far as the basic logic function is concerned, the additional transistors are unnecessary. However, the "buffering" they provide does serve a useful function. What is that function? Are there any disadvantages to buffered logic gates, versus unbuffered?

file 01280

Question 30

In the early days of solid-state logic gate circuit technology, there was a very clear distinction between TTL and CMOS. TTL gates were capable of switching on and off very fast, required a tightly regulated power supply voltage, and used a lot of power. CMOS gates were not quite as fast as TTL, but could tolerate a much wider range of power supply voltages and were far less wasteful on power.

Then, during the 1980's a new technology known as *high-speed CMOS*, or HCMOS, entered the scene. Explain what HCMOS is, how it compares to the older TTL and CMOS families (54/74xx and 4xxx number series, respectively), and where it is often used. Hint: high-speed CMOS bears the same numerical codes as the old TTL 54xx and 74xx series ICs (e.g. 74HC00 instead of 7400).

file 02773

Question 31

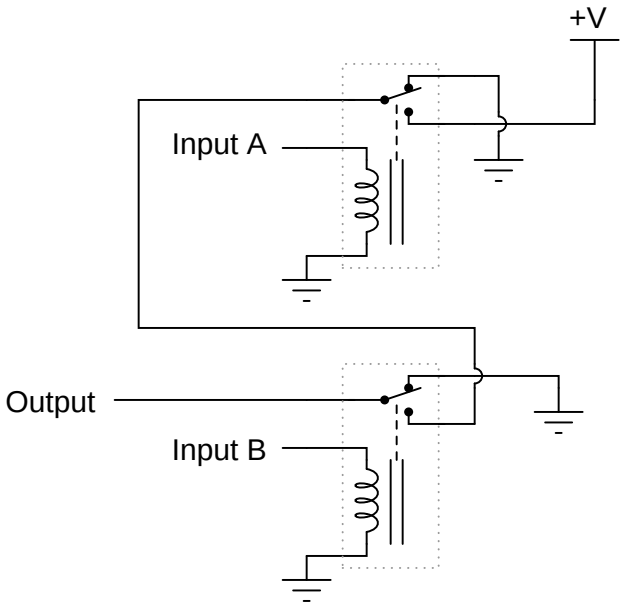
Though many electronics students and professionals alike associate semiconductor components with the word "digital," electromechanical relays are also digital logic (on or off) devices. In fact, some of the first digital computers were built with electromechanical relays as their active elements.

In what ways are electromechanical relays similar to semiconductor logic gates? In what ways do the two digital technologies differ?

file 01287

Question 32

The following schematic is of a relay circuit that emulates a standard digital logic gate function:

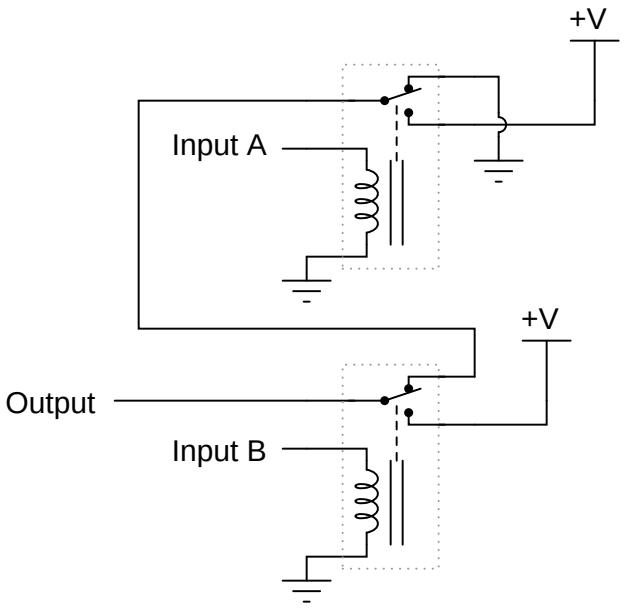


Write a truth table for this circuit's function, and determine what name best represents it (AND, OR, NAND, NOR, or NOT).

file 01288

Question 33

The following schematic is of a relay circuit that emulates a standard digital logic gate function:

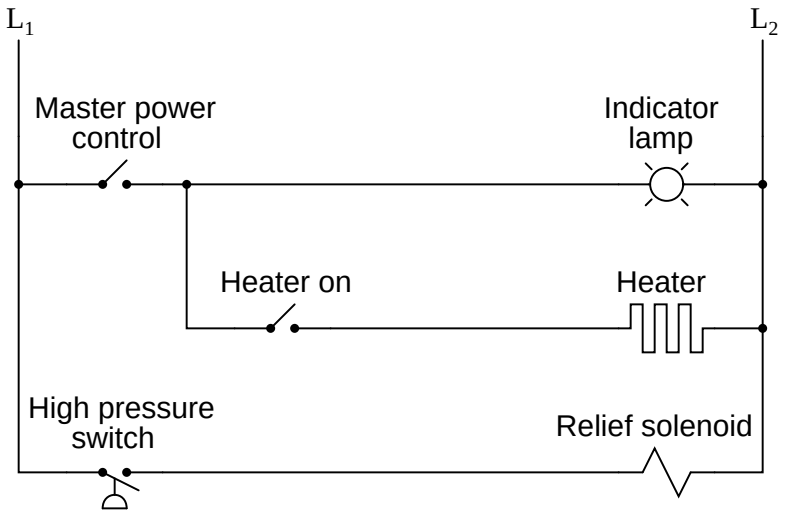


Write a truth table for this circuit's function, and determine what name best represents it (AND, OR, NAND, NOR, or NOT).

file 01289

Question 34

A type of electrical diagram convention optimal for representing electromechanical relay circuits is the *ladder logic diagram*. An example of a "ladder logic" diagram is shown here:



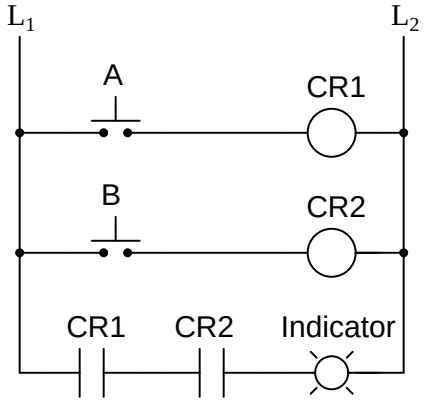
Each parallel circuit branch is represented as its own horizontal "rung" between the two vertical "rails" of the ladder. As you may have noticed, some of the symbols resemble standard electrical/electronic schematic symbols (toggle switches, for instance), while others are unique to ladder logic diagrams (heater elements, solenoid coils, lamps).

Where do the circuits shown obtain their electrical power? What do "L1" and "L2" represent? How are relay coils and contacts represented in a ladder logic diagram? Answer each of these questions by expanding upon the diagram shown above: draw the components necessary to show a complete electrical circuit (i.e. details of the power source), as well as an additional rung (or two) showing a relay coil actuated by some sort of switch contact, and the relay contact controlling power to a second indicator lamp.

file 01290

Question 35

In ladder logic symbolism, an electromechanical relay coil is shown as a circle, and the contact(s) actuated by the coil as two parallel lines, almost like a capacitor symbol. Given this knowledge, interpret the following ladder logic diagram:



How do we know which relay contact is actuated by which relay coil? How does this convention differ from that of standard electrical/electronic schematic diagrams, where the relay coil is shown as an actual coil of wire (inductor symbol) with the contact "linked" to the coil by a dashed line? Also, what type of logic function behavior (AND, OR, NAND, or NOR) does the above circuit exhibit?

file 02774

Question 36

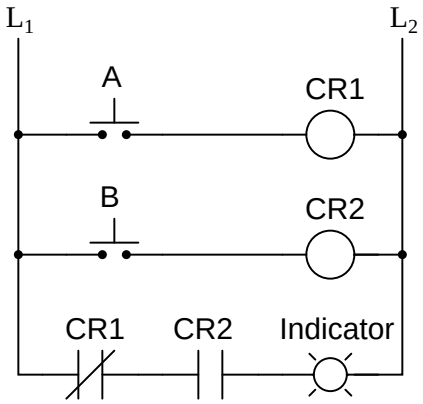
Complete the following ladder logic diagram so that an OR gate function is formed: the indicator lamp energizes if either switch A *or* switch B is actuated.

file 01293

Question 37

In ladder logic diagrams, a normally-open relay contact is drawn as a set of parallel lines, almost like a non-polarized capacitor in an electronic schematic diagram. Normally-closed relay contacts differ in symbolism by having a diagonal line drawn through them.

Analyze the following relay logic circuit, completing the truth table accordingly:



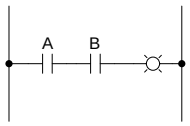
Truth table

A	B	Output
0	0	
0	1	
1	0	
1	1	

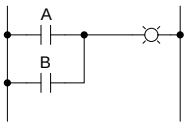
file 02775

Question 38

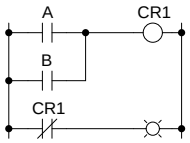
Identify each of these relay logic functions by name (AND, OR, NOR, etc.) and complete their respective truth tables:



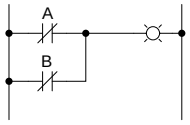
A	B	Output
0	0	
0	1	
1	0	
1	1	



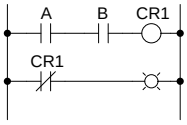
A	B	Output
0	0	
0	1	
1	0	
1	1	



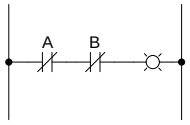
A	B	Output
0	0	
0	1	
1	0	
1	1	



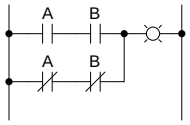
A	B	Output
0	0	
0	1	
1	0	
1	1	



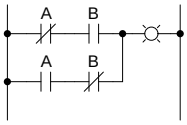
A	B	Output
0	0	
0	1	
1	0	
1	1	



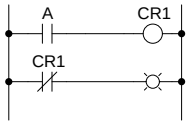
A	B	Output
0	0	
0	1	
1	0	
1	1	



A	B	Output
0	0	
0	1	
1	0	
1	1	



A	B	Output
0	0	
0	1	
1	0	
1	1	

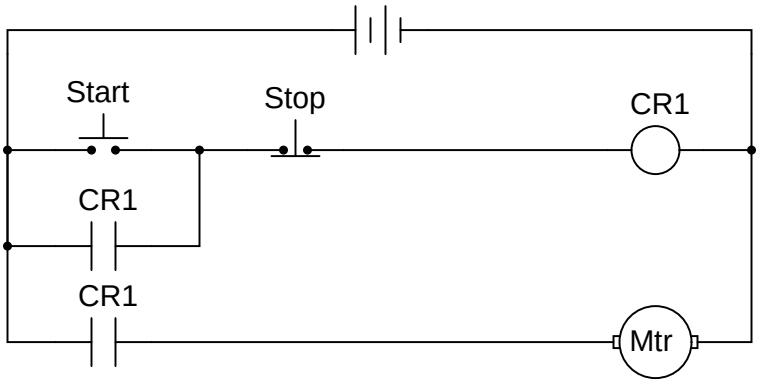


A	Output
0	
1	

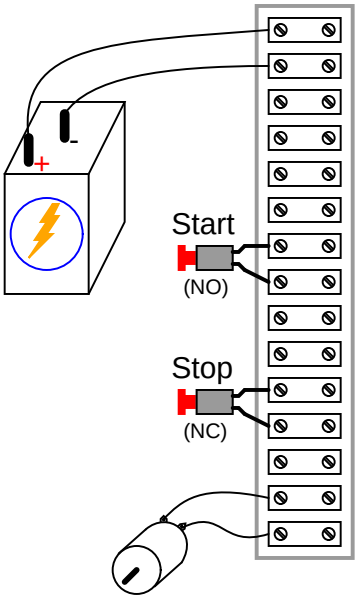
file 01335

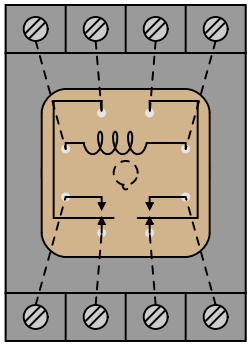
Question 39

A *very* common application of electromechanical relay logic is motor control circuitry. Here is a ladder diagram for a simple DC motor control, where a momentary pushbutton switch starts the motor, and another pushbutton switch stops the motor:



Translate this ladder diagram into point-to-point connections between the following components (shown in the following illustration):



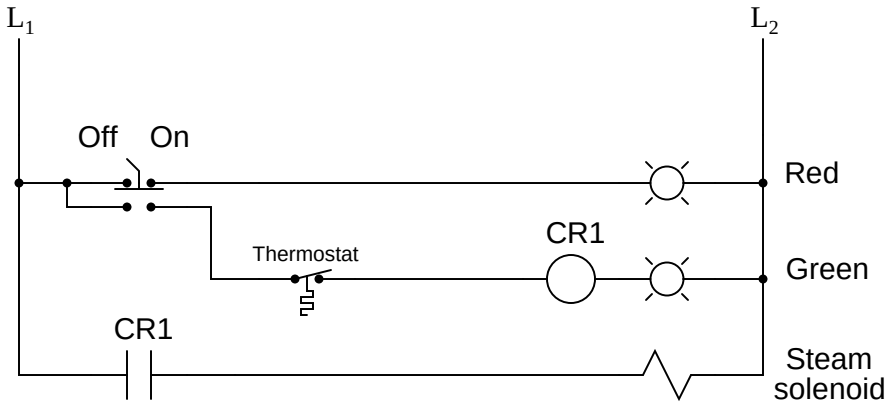


(Dashed lines represent connections between relay terminals and socket screw lugs, hidden from sight)

file 01295

Question 40

The following ladder logic diagram (for a steam heater control) contains a serious mistake:

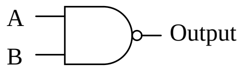


This is a mistake I've seen many students make. Explain what the mistake is, and draw a corrected version of this relay circuit.

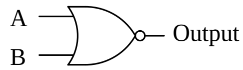
file 01350

Question 41

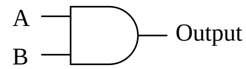
Identify each of these logic gates by name, and complete their respective truth tables:



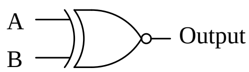
A	B	Output
0	0	
0	1	
1	0	
1	1	



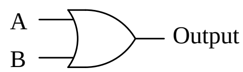
A	B	Output
0	0	
0	1	
1	0	
1	1	



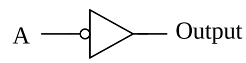
A	B	Output
0	0	
0	1	
1	0	
1	1	



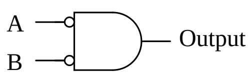
A	B	Output
0	0	
0	1	
1	0	
1	1	



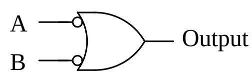
A	B	Output
0	0	
0	1	
1	0	
1	1	



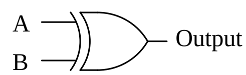
A	Output
0	
1	



A	B	Output
0	0	
0	1	
1	0	
1	1	



A	B	Output
0	0	
0	1	
1	0	
1	1	



A	B	Output
0	0	
0	1	
1	0	
1	1	

file 02776

Question 42

Totem-pole TTL gates usually differ greatly in their maximum source current versus maximum sink current (I_{OH} versus I_{OL}). Identify which current rating is usually greater, and also explain why this is.

file 01667

Question 43

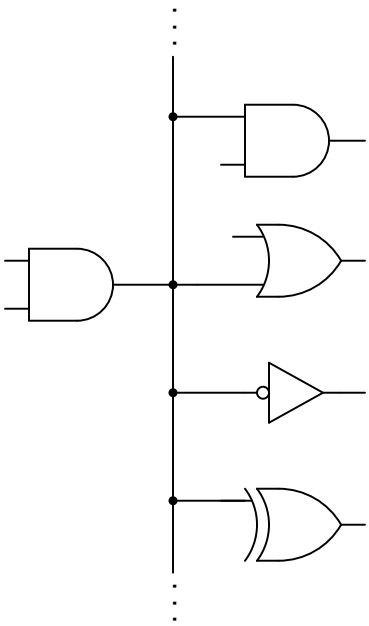
In high-speed digital circuits, a very important logic gate parameter is *propagation delay*: the delay time between a change-of-state on a gate's input and the corresponding change-of-state on that gate's output. Consult a manufacturer's datasheet for any TTL logic gate and report the typical propagation delay times published there.

Also, explain what causes propagation delay in logic gates. Why isn't the change in output state instantaneous when an input changes states?

file 01264

Question 44

Logic gates are limited in the number of gate inputs which one output can reliably drive. This limit is referred to as *fan-out*:



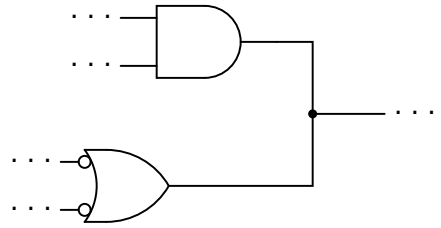
Explain why this limit exists. What is it about the construction of TTL logic gates that inherently limits the number of TTL inputs that any one TTL output can drive? What might happen if this limit is exceeded?

Locate a datasheet for a TTL gate and research its fan-out limit. Note: this number will vary with the particular type of TTL referenced (L, LS, H, AS, ALS, etc.).

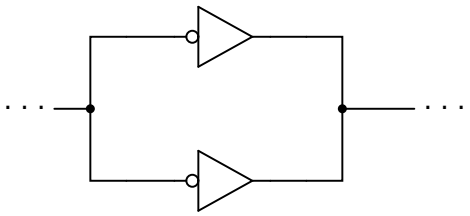
file 01267

Question 45

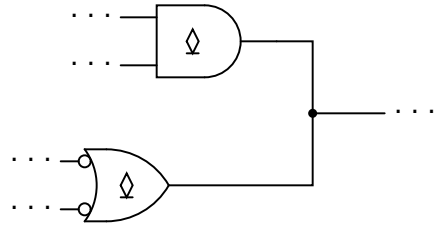
Explain why it is generally a *very bad* design practice to connect the outputs of different logic gates together, like this:



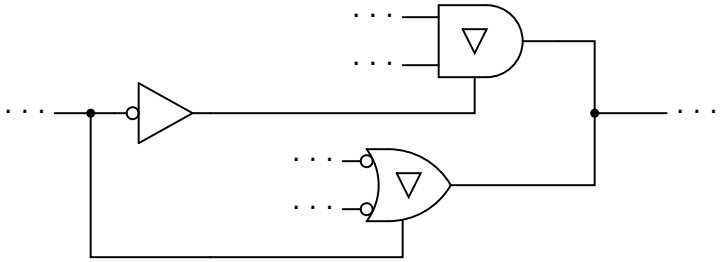
However, there are certain specific circumstances in which "paralleling" gate outputs is acceptable. For instance, it is okay to parallel two or more inverters, like this:



No damage will be done if open-collector gate outputs are paralleled, either (although the resulting logic function may be strange):



And finally, gates that have *tri-state* outputs may also have their outputs paralleled if certain precautions are taken:



What, specifically, causes gates to be damaged by "paralleling" their outputs? Generally speaking, what principle must be followed in order to "parallel" logic gate outputs without risk of damage? Explain how each of the three acceptable "paralleled" scenarios shown here meet this criterion.

Suggestion: the issue of multiple gates having to output logic voltage signals onto common conductors ("busses") is called *bus contention*. Try looking for this term in your research to see what useful information you find on paralleled gates!

file 01282

Question 46

An important parameter of logic gate circuitry is *noise margin*. What exactly is "noise margin," and how is it defined for logic gates?

Specifically, how much noise margin do digital circuits exclusively composed of TTL gates have?

Note: you will need to consult TTL gate datasheets to answer this question properly.

file 01269

Question 47

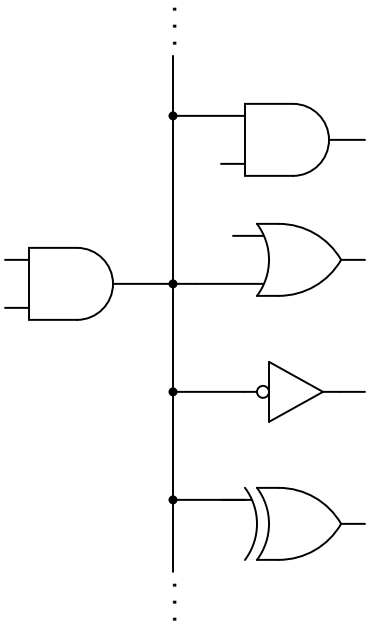
In high-speed digital circuits, a very important logic gate parameter is *propagation delay*: the delay time between a change-of-state on a gate's input and the corresponding change-of-state on that gate's output. Consult a manufacturer's datasheet for any CMOS logic gate and report the typical propagation delay times published there.

Also, explain what causes propagation delay in logic gates. Why isn't the change in output state instantaneous when an input changes states?

file 01276

Question 48

Logic gates are limited in the number of gate inputs which one output can reliably drive. This limit is referred to as *fan-out*:



Explain why this limit exists. What is it about the construction of CMOS logic gates that inherently limits the number of CMOS inputs that any one CMOS output can drive? What might happen if this limit is exceeded?

Fan-out for CMOS is a quite different than fan-out for TTL. Most importantly is that CMOS fan-out is inversely proportional to operating frequency. Explain why.

file 01268

Question 49

An important parameter of logic gate circuitry is *noise margin*. What exactly is "noise margin," and how is it defined for logic gates?

Specifically, how much noise margin do digital circuits exclusively composed of CMOS gates have? How does this compare with the noise margin of all-TTL circuitry?

Note: you will need to consult CMOS gate datasheets to answer this question properly.

file 01270

Question 50

A trend in CMOS logic gate development is toward lower and lower operating voltages. The "AUC" family of CMOS logic, for example, is able to operate at less than 2 volts V_{DD}!

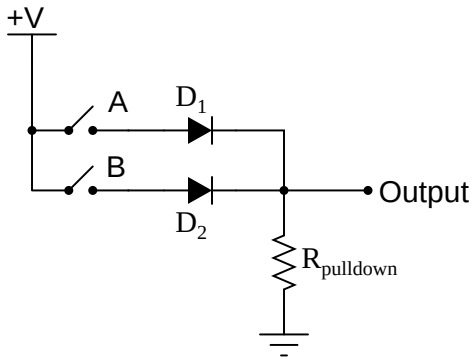
Explain why this is a trend in modern logic circuit design. What benefits result from lower operating voltages? What possible disadvantages also result?

file 01279

Question 51

Competency: **OR gate, diode-resistor logic** Version:

Schematic



Given conditions

V_{DD} = $R_{pulldown}$ =

Truth table

Predicted

A	B	Output
0	0	
0	1	
1	0	
1	1	

Actual

A	B	Output
0	0	
0	1	
1	0	
1	1	

Fault analysis

Suppose component [ ] fails ☐ open ☐ other _____ ☐ shorted

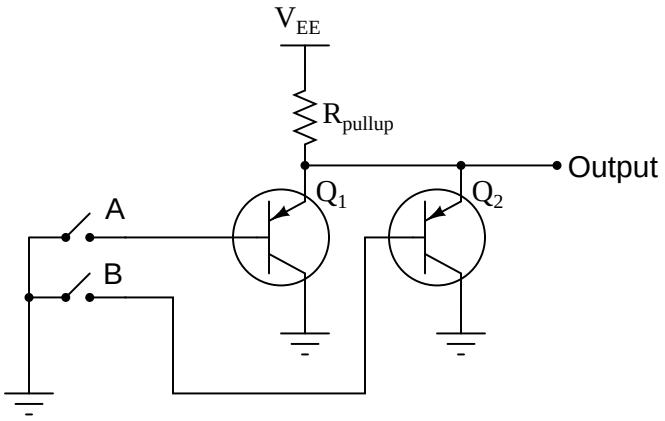
What will happen in the circuit?

file 02787

Question 52

Competency: **AND gate, simple BJT logic** Version:

Schematic



Given conditions

V_{EE} = R_{pullup} =

Truth table

Predicted

A	B	Output
0	0	
0	1	
1	0	
1	1	

Actual

A	B	Output
0	0	
0	1	
1	0	
1	1	

Fault analysis

Suppose component [ ] fails ☐ open ☐ other _____ ☐ shorted

What will happen in the circuit?

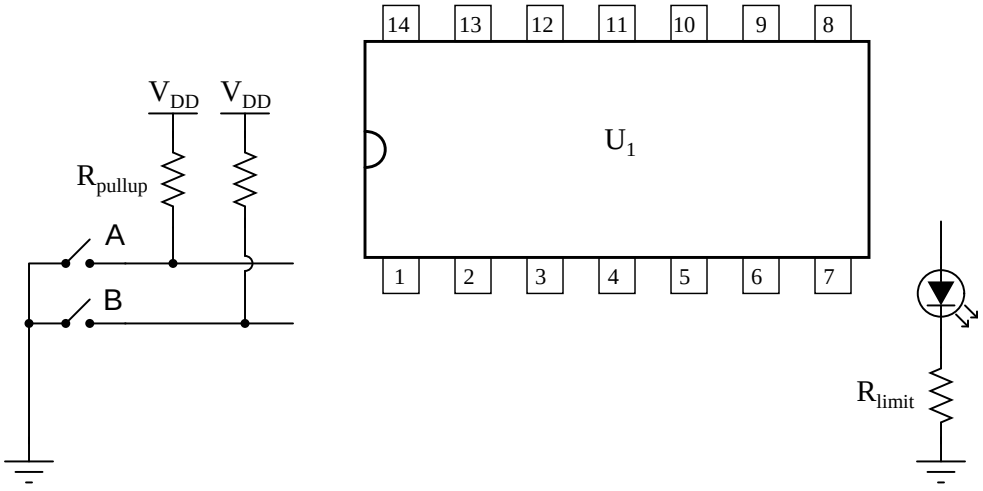
file 02793

Competency: **IC logic gate usage** Version:

Description

Connect one of the IC's two-input gates to the switches and to the LED, then prove your prediction for that gate's truth table.

Diagram



Given conditions *(instructor chooses IC part number)*

V_{DD} = R_{pullup} = R_{limit} = U_1 =

Truth table

Predicted

A	B	Output
0	0	
0	1	
1	0	
1	1	

Actual

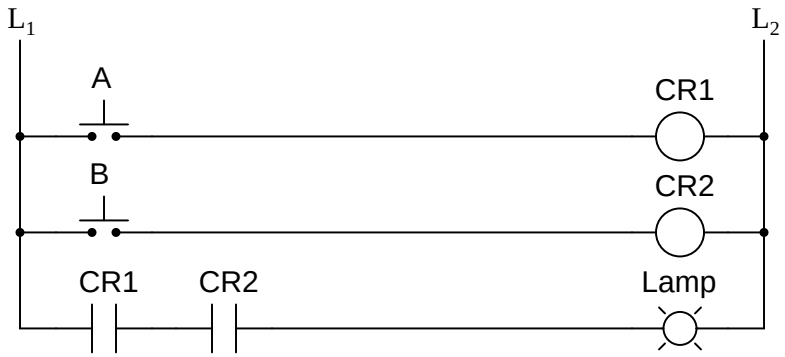
A	B	Output
0	0	
0	1	
1	0	
1	1	

file 02789

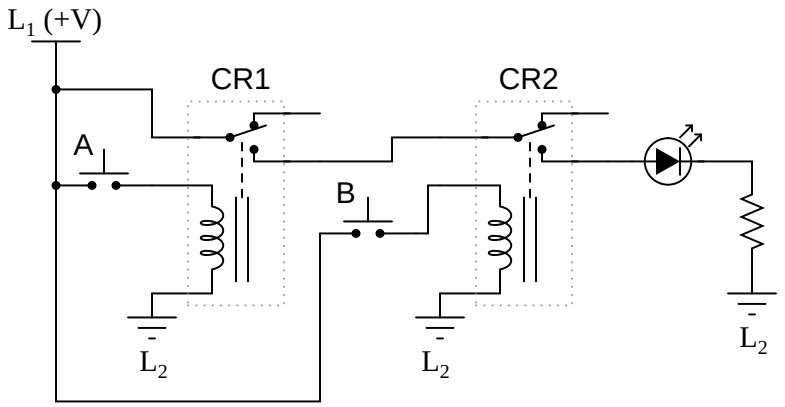
Question 54

Competency: **AND gate, relay logic** Version:

Ladder logic diagram



Schematic



Truth table

Predicted

A	B	Output
0	0	
0	1	
1	0	
1	1	

Actual

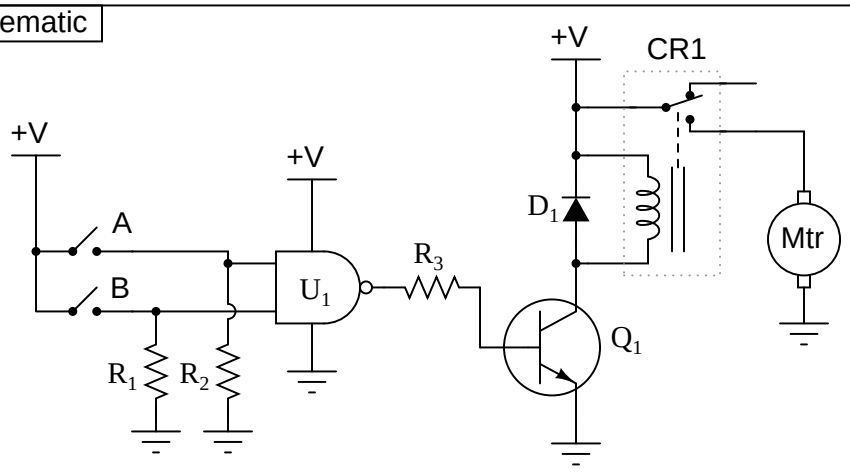
A	B	Output
0	0	
0	1	
1	0	
1	1	

file 02791

Question 55

Competency: **Gate-relay interposing** Version:

Schematic



Given conditions

+V = $R_1 = R_2$ = R_3 =

Truth table

Predicted

A	B	Output
0	0	
0	1	
1	0	
1	1	

Actual

A	B	Output
0	0	
0	1	
1	0	
1	1	

Fault analysis

Suppose component [ ] fails ☐ open ☐ other _____ ☐ shorted

What will happen in the circuit?

file 02795

Question 56

NAME: _____ **Project Grading Criteria** PROJECT: _____

You will receive the highest score for which *all* criteria are met.

100 % *(Must meet or exceed all criteria listed)*

A. Impeccable craftsmanship, comparable to that of a professional assembly
B. No spelling or grammatical errors anywhere in *any* document, upon first submission to instructor

95 % *(Must meet or exceed these criteria in addition to all criteria for 90% and below)*

A. Technical explanation sufficiently detailed to teach from, inclusive of every component (supersedes 75.B)
B. Itemized parts list complete with part numbers, manufacturers, and (equivalent) prices for *all* components, including recycled components and parts kit components (supersedes 90.A)

90 % *(Must meet or exceed these criteria in addition to all criteria for 85% and below)*

A. Itemized parts list complete with prices of components purchased for the project, plus total price
B. No spelling or grammatical errors anywhere in *any* document upon final submission

85 % *(Must meet or exceed these criteria in addition to all criteria for 80% and below)*

A. "User's guide" to project function (in addition to 75.B)
B. Troubleshooting log describing all obstacles overcome during development and construction

80 % *(Must meet or exceed these criteria in addition to all criteria for 75% and below)*

A. All controls (switches, knobs, etc.) clearly and neatly labeled
B. All documentation created on computer, not hand-written (including the schematic diagram)

75 % *(Must meet or exceed these criteria in addition to all criteria for 70% and below)*

A. Stranded wire used wherever wires are subject to vibration or bending
B. Basic technical explanation of all major circuit sections
C. Deadline met for working prototype of circuit (Date/Time = _____ / _____)

70 % *(Must meet or exceed these criteria in addition to all criteria for 65%)*

A. All wire connections sound (solder joints, wire-wrap, terminal strips, and lugs are all connected properly)
B. No use of glue where a fastener would be more appropriate
C. Deadline met for submission of fully-functional project (Date/Time = _____ / _____) – supersedes 75.C if final project submitted by that (earlier) deadline

65 % *(Must meet or exceed these criteria in addition to all criteria for 60%)*

A. Project fully functional
B. All components securely fastened so nothing is "loose" inside the enclosure
C. Schematic diagram of circuit

60 % *(Must meet or exceed these criteria in addition to being safe and legal)*

A. Project minimally functional, with all components located inside an enclosure (if applicable)
B. Passes final safety inspection (proper case grounding, line power fusing, power cords strain-relieved)

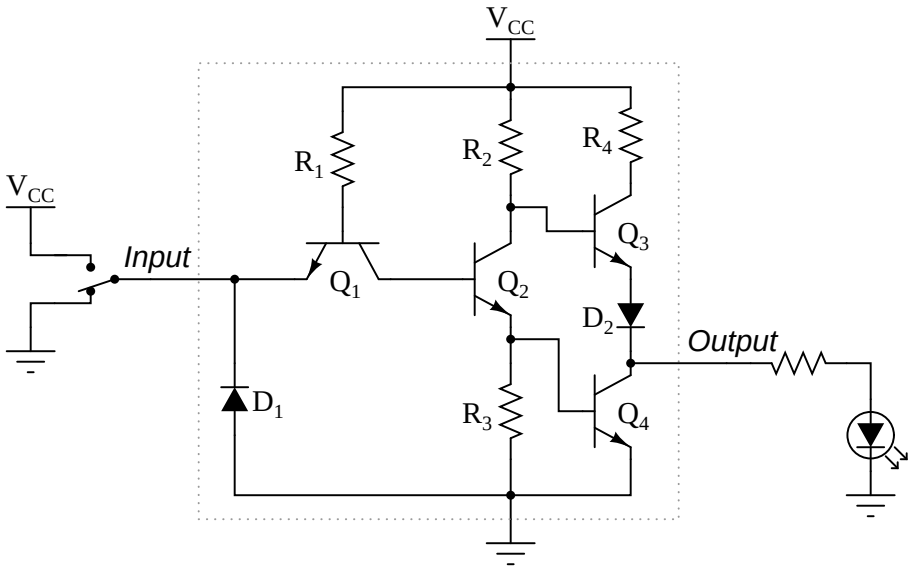
0 % *(If any of the following conditions are true)*

A. Fails final safety inspection (improper grounding, fusing, and/or power cord strain relieving)
B. Intended project function poses a safety hazard
C. Project function violates any law, ordinance, or school policy

file 03173

Question 57

Predict how the operation of this logic gate circuit will be affected as a result of the following faults. Consider each fault independently (i.e. one at a time, no multiple faults):

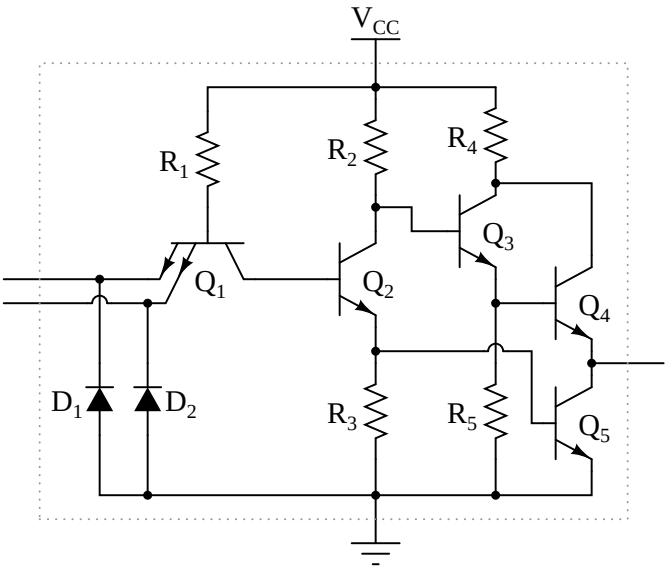


- Diode D_1 fails open:
- Diode D_1 fails shorted:
- Diode D_2 fails open:
- Resistor R_1 fails open:
- Resistor R_2 fails open:
- Resistor R_4 fails open:

For each of these conditions, explain *why* the resulting effects will occur.
file 03822

Question 58

Predict how the operation of this logic gate circuit will be affected as a result of the following faults. Consider each fault independently (i.e. one at a time, no multiple faults):

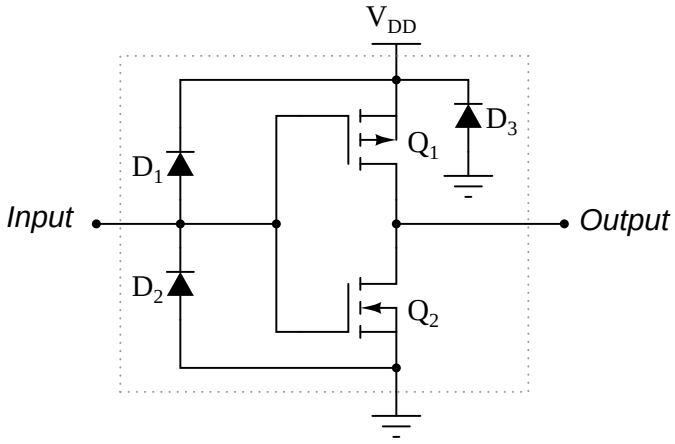


- Diode D_1 fails open:
- Diode D_1 fails shorted:
- Diode D_2 fails open:
- Resistor R_1 fails open:
- Resistor R_2 fails open:
- Transistor Q_2 emitter terminal fails open:
- Transistor Q_3 emitter terminal fails open:

For each of these conditions, explain *why* the resulting effects will occur.
file 03823

Question 59

Predict how the operation of this logic gate circuit will be affected as a result of the following faults. Consider each fault independently (i.e. one at a time, no multiple faults):

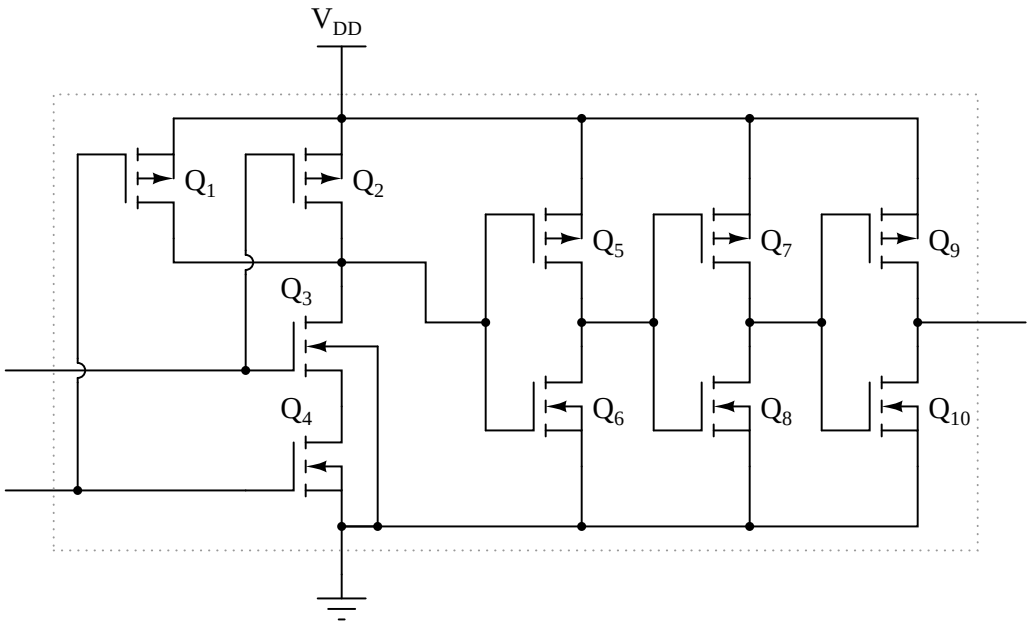


- Diode D_1 fails open:
- Diode D_1 fails shorted:
- Diode D_2 fails open:
- Diode D_2 fails shorted:
- Transistor Q_1 fails open (drain to source):
- Transistor Q_2 fails open (drain to source):

For each of these conditions, explain *why* the resulting effects will occur.
file 03824

Question 60

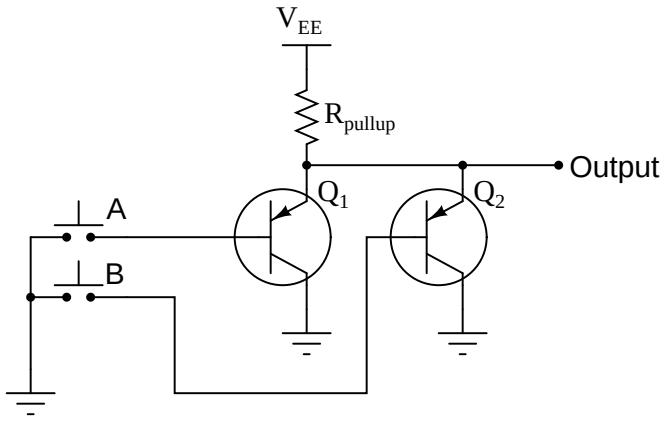
Identify at least three different transistor faults in this CMOS logic gate that could cause the output to fail *low*:



file 03825

Question 61

Identify at least two faults in this simple logic gate circuit that could cause its output to fail in the "low" logic state:

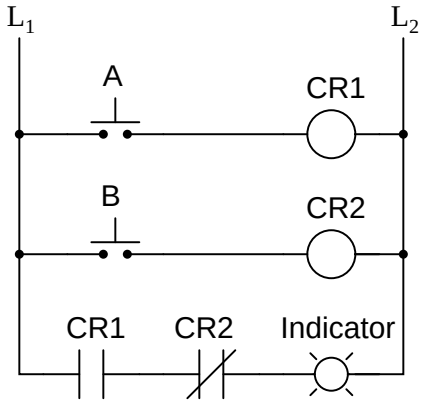


Be sure to explain *why* the proposed faults would cause the output to fail low.

file 03830

Question 62

Complete the truth table for the following relay logic circuit, and then complete a second truth table for the same circuit with relay coil CR2 failed open:



Truth table (good circuit)

A	B	Output
0	0	
0	1	
1	0	
1	1	

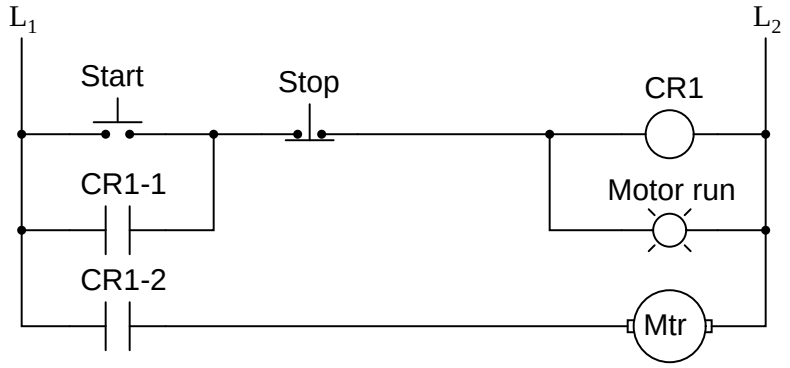
Truth table (with fault)

A	B	Output
0	0	
0	1	
1	0	
1	1	

Explain *why* the truth table will be modified as a result of the fault.
file 03826

Question 63

Predict how the operation of this motor control circuit will be affected as a result of the following faults. Consider each fault independently (i.e. one at a time, no multiple faults):

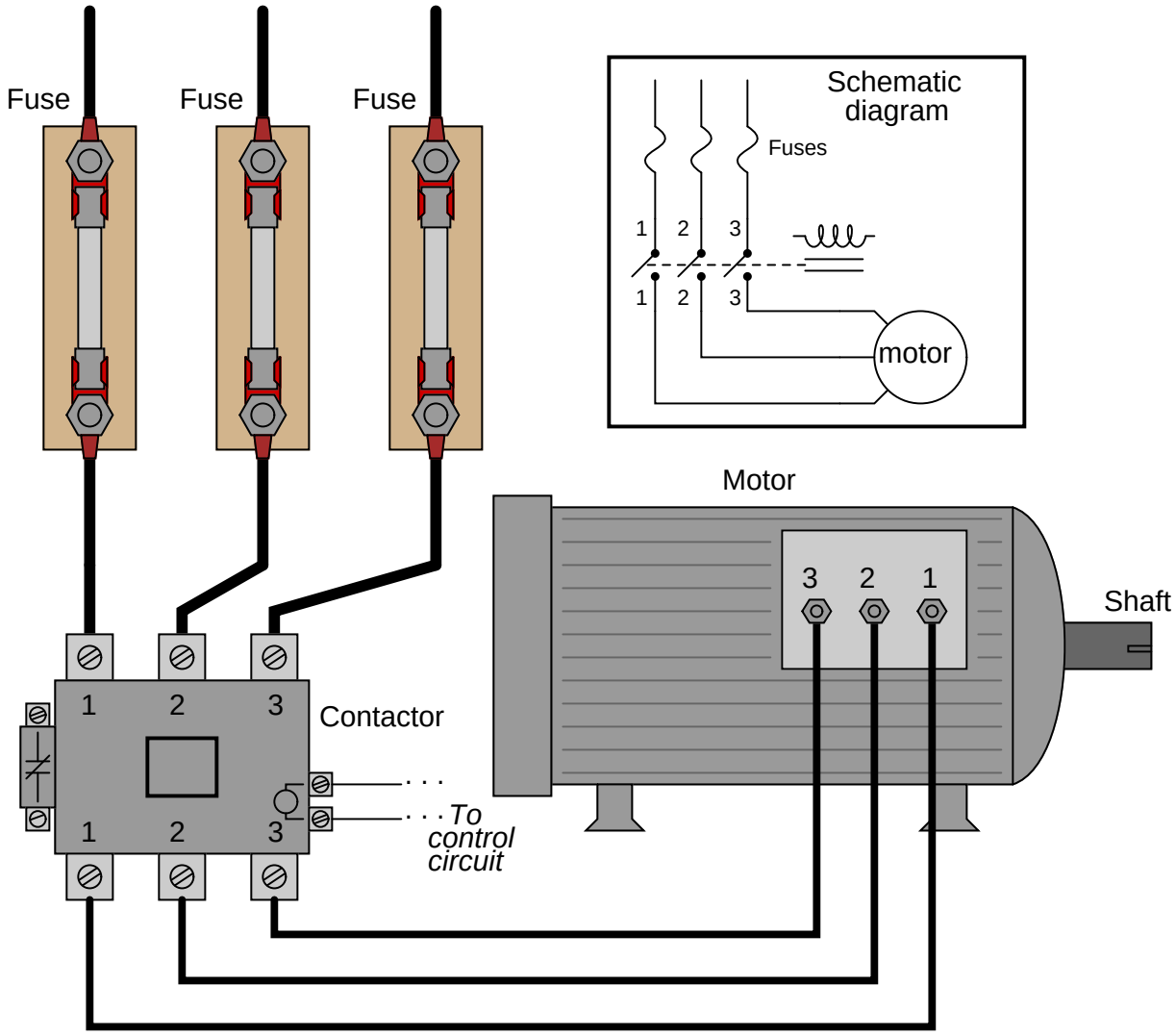


- "Stop" pushbutton switch fails open:
- Relay contact CR1-1 fails open:
- Relay contact CR1-2 fails open:
- Relay coil CR1 fails open:

For each of these conditions, explain *why* the resulting effects will occur.
file 03827

Question 64

There is something wrong in this motor control circuit. When the start button is pressed, the contactor energizes but the motor itself does not run:

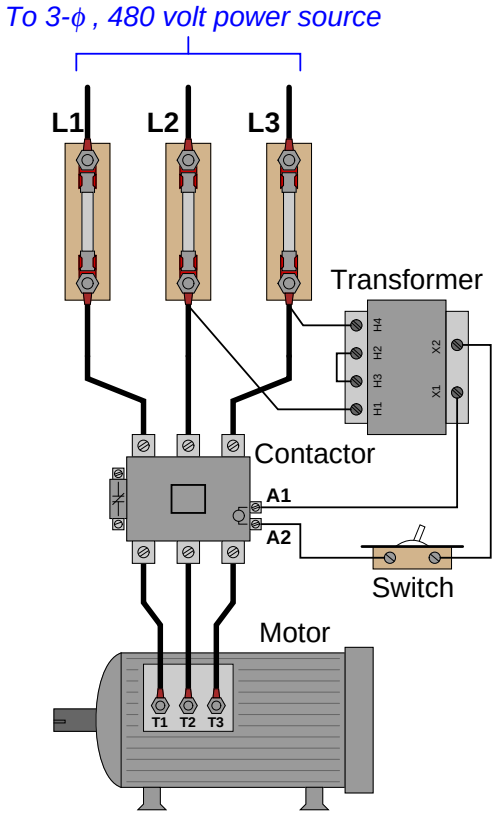


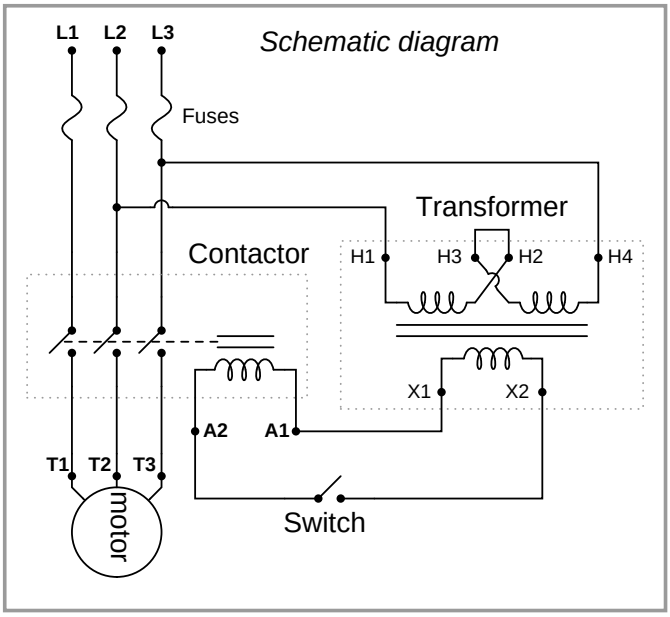
Identify a good place to check with your multimeter to diagnose the nature of the fault, and explain your reasoning.

file 03828

Question 65

Identify at least three independent faults that could cause this motor not to start:



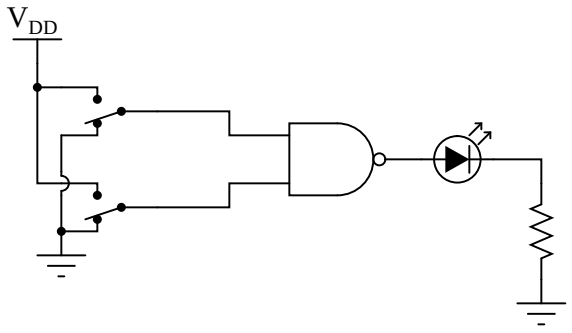


For each of the proposed faults, explain *why* they would prevent the motor from starting.

file 03829

Question 66

A student builds the following circuit to demonstrate the behavior of a NAND gate:



When the student tests the circuit, though, something is wrong:

- Both switches LOW, no light.
- One switch HIGH, the other switch LOW; LED lights up.
- One switch LOW, the other switch HIGH; LED lights up.
- Both switches HIGH, no light.

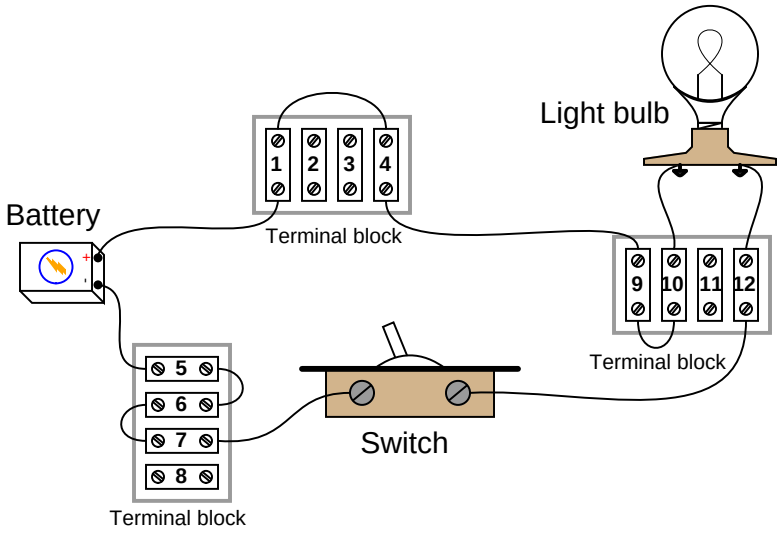
Instead of acting as a NAND gate should, it seems to behave as if it were an Exclusive-OR gate! Examining the circuit for mistakes, the student discovers missing power connections to the chip – in other words, neither V_{DD} nor V_{SS} are connected to the power source.

While this certainly is a problem, the student is left to wonder, "How did the circuit ever function *at all*?" With no power connected to the chip, how is it possible that the LED ever lit in *any* condition?

file 01561

Question 67

Examine the following illustration of a simple battery-switch-lamp circuit, connected together using screw-terminal blocks, each connection point on each terminal block identified by a unique number:



Determine whether or not voltage should be present between the following pairs of terminal block points with the switch in the ON position:

- Points 1 and 5:
- Points 6 and 7:
- Points 4 and 10:
- Points 9 and 12:
- Points 6 and 12:
- Points 9 and 10:
- Points 4 and 7:

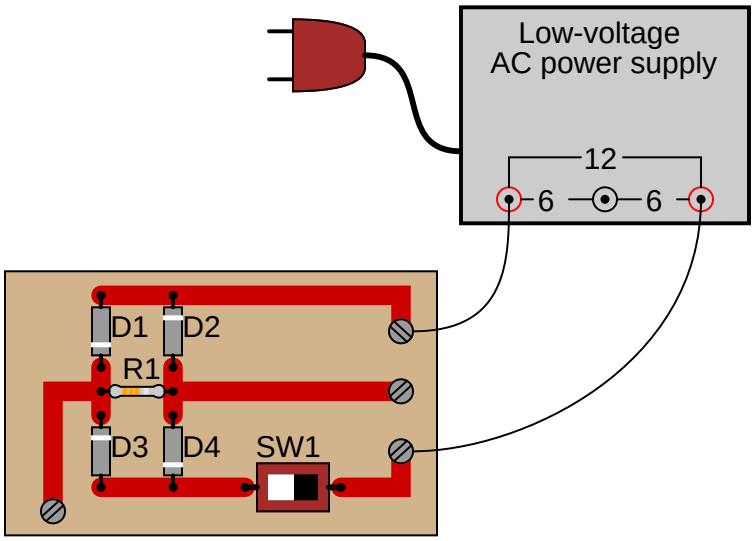
Now, determine whether or not voltage should be present between the following pairs of terminal block points with the switch in the OFF position:

- Points 1 and 5:
- Points 6 and 7:
- Points 4 and 10:
- Points 9 and 12:
- Points 6 and 12:
- Points 9 and 10:
- Points 4 and 7:

file 03302

Question 68

The circuit shown here is called a "bridge rectifier," and its purpose is to convert alternating current (from the "power-supply" unit) into direct current. Suppose you were instructed to check the continuity of the switch (SW1) mounted on the printed circuit board. What would be a fast and effective way of testing this switch's continuity (ideally, without removing the switch from the circuit board)?



file 00100

Question 69

Identify which of these are true statements:

1. Between two points that are electrically common to each other, there is guaranteed to be zero voltage.
2. If zero voltage is measured between two points, those points must be electrically common to each other.
3. Between two points that are not electrically common to each other, there is guaranteed to be voltage.
4. If voltage is measured between two points, those points must not be electrically common to each other.

file 00184

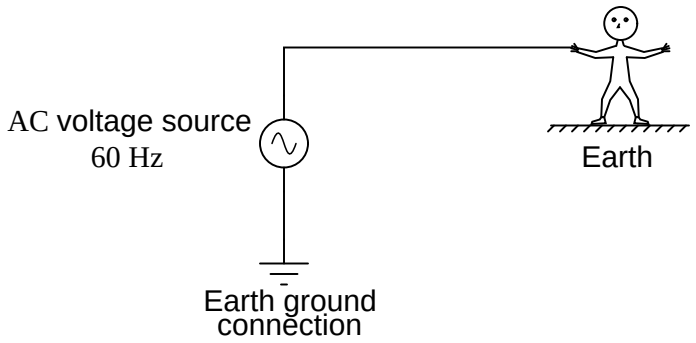
Question 70

An American researcher named Charles Dalziel performed experiments with both human and animal subjects to determine the effects of electric currents on the body. A table showing his research data is presented here:

Bodily effect	*Gender*	*DC*	*60 Hz AC*	*10 kHz AC*
Slight sensation at point(s) of contact	Men	1 mA	0.4 mA	7 mA
	Women	0.6 mA	0.3 mA	5 mA
Threshold of bodily perception	Men	5.2 mA	1.1 mA	12 mA
	Women	3.5 mA	0.7 mA	8 mA
Pain, with voluntary muscle control maintained	Men	62 mA	9 mA	55 mA
	Women	41 mA	6 mA	37 mA
Pain, with loss of voluntary muscle control	Men	76 mA	16 mA	75 mA
	Women	51 mA	10.5 mA	50 mA
Severe pain, difficulty breathing	Men	90 mA	23 mA	94 mA
	Women	60 mA	15 mA	63 mA
Possible heart fibrillation after three seconds	Men	500 mA	100 mA	
	Women	500 mA	100 mA	

Important Note: *Dalziel's human test subjects were men and women in good health, with no known heart conditions or any other abnormalities that would have compromised their safety. In other words, these data points represent best-case scenarios, and do not necessarily reflect the risk to persons in poorer states of health.*

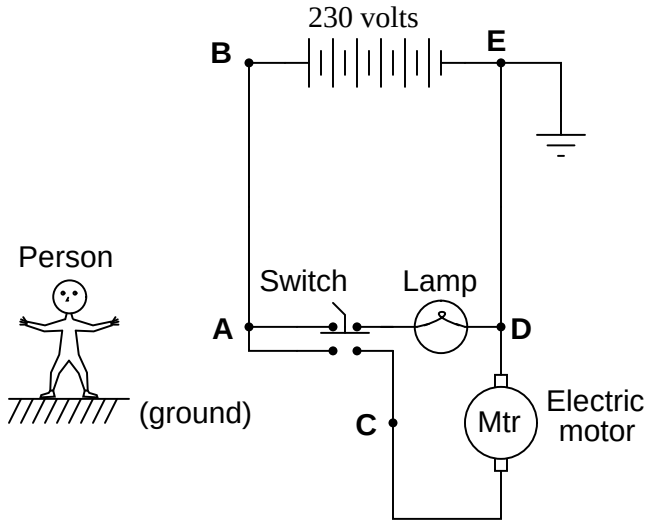
Assuming a wire-to-hand contact resistance of 1500 Ω, 4400 Ω of resistance for foot-to-ground contact, 50 Ω internal body resistance, 200 Ω of resistance through the soil from the person's location to the earth ground point, and a female victim, calculate the amount of voltage necessary to achieve each of the listed shock conditions (threshold of perception, pain, etc.) for the following circuit:



file 03246

Question 71

Determine whether or not a shock hazard exists for a person standing on the ground, by touching any one of the points labeled in this circuit:



- Point "A"
- Point "B"
- Point "C"
- Point "D"
- Point "E"

file 00303

Question 72

The following recommendations came from a flyer published by an electric power utility. Read and comment on their instructions regarding downed power lines:

> *Assume any downed line is an energized power line. If a power line falls on your car while you are driving, slowly drive on until you are completely clear of the line (but do not drive over it). If your car is immobilized, stay in it until help arrives. Call for help from a cell phone if you have one.*
>
> *If you need to escape from a vehicle, such as for a car fire, jump clear of the car. Electricity is not only traveling through the vehicle, but may also be traveling in the ground around the area. Keep your arms crossed over your chest while you jump, and both feet together. Do NOT touch the vehicle and the ground at the same time. Once you land on the ground, shuffle clear of the area, keeping both feet together, on the ground, and touching at all times. Continue shuffling until you're at least 30 feet from the accident site.*

Why do you suppose the following actions were recommended?

- Do not drive over a downed power line.
- Stay in the car if possible.
- Do not touch the car and the ground at the same time.
- Shuffle away from the car (rather than walk), with both feet together.

file 02911

Question 73

When securing equipment for safe maintenance, special *tags* are attached with the lock(s) used to keep circuit breakers and other disconnect devices in the open (off) state. A typical "lockout" tag looks something like this:

What is the purpose of attaching such a tag to an electrical disconnect device in addition to locking it in the open position? Why is a lock, by itself, not sufficient from a safety perspective?

file 00573

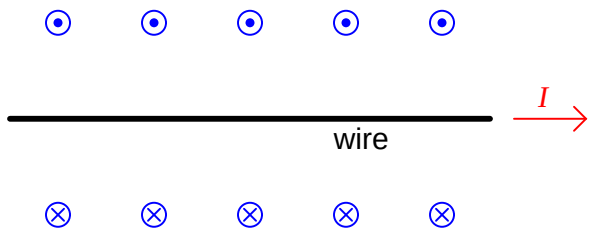
Question 74

Suppose you are finishing a maintenance project where an electric motor was locked out and tagged, and now the work is complete. Your lock is the last one to be removed from the circuit breaker, everyone else already having taken their locks and tags off. What should you do before removing your lock and turning the circuit breaker back on?

file 00575

Question 75

When engineers and physicists draw pictures illustrating the magnetic field produced by a straight current-carrying wire, they usually do so using this notation:

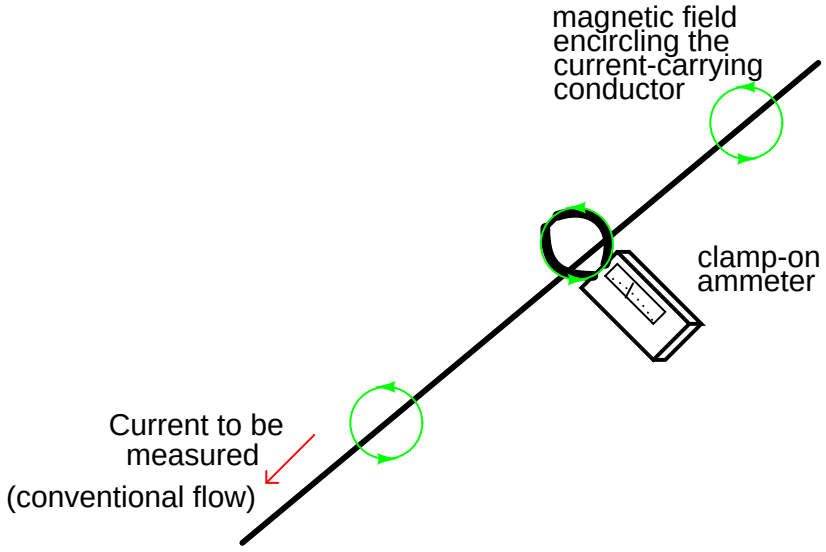


Explain what the circle-and-dot and circle-and-cross symbols mean, with reference to the *right-hand rule*.

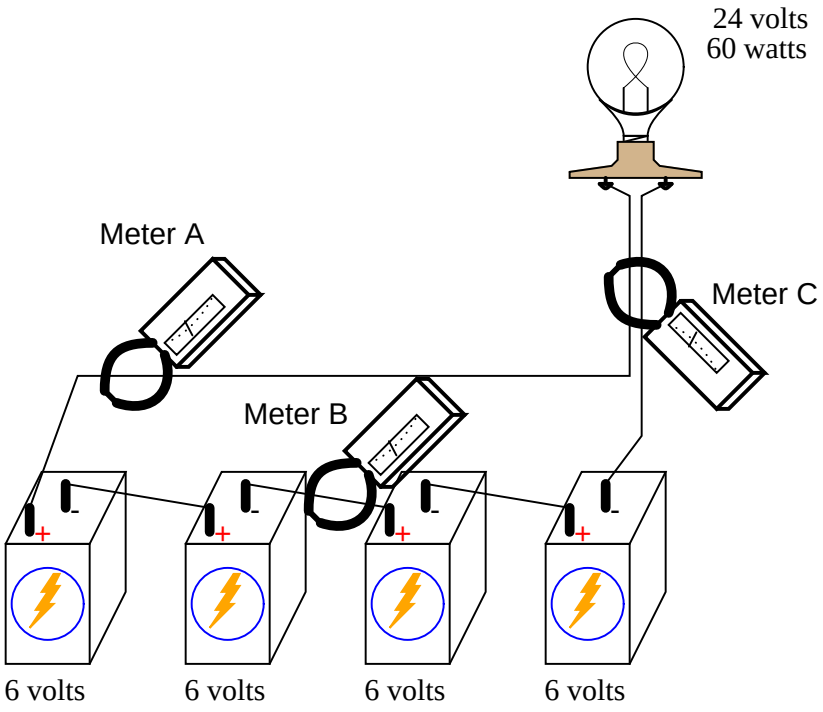
file 03498

Question 76

A very useful method of measuring current through a wire is to measure the strength of the magnetic field around it. This type of ammeter is known as a *clamp-on* ammeter:



Knowing the principle behind this meter's operation, describe what current values will be indicated by the three clamp-on ammeters in this circuit:



- Meter A =
- Meter B =
- Meter C =

file 00262

Question 77

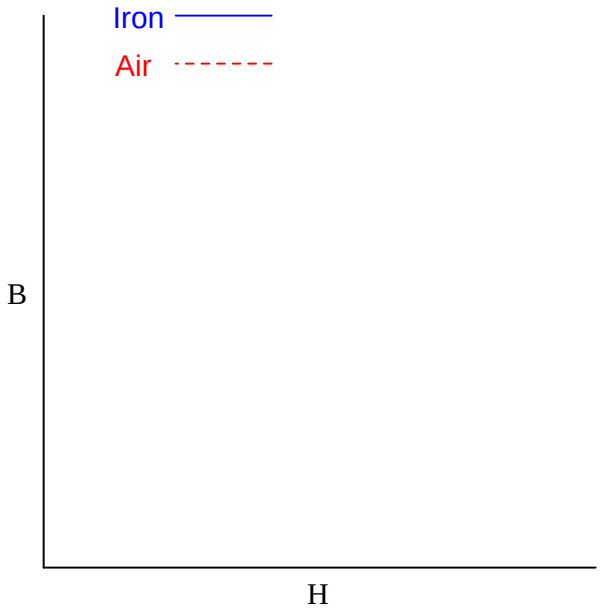
Write an equation that expresses the amount of magnetic flux (Φ) produced by an electromagnet, given the amount of electric current (I), the number of turns in the wire coil (N), and the reluctance of the core material ($\Re$).

file 00258

Question 78

$\int f(x)\,dx$ *Calculus alert!*

Plot the relative B-H curves for a sample of air and a sample of iron, in proportion to each other (as much as possible):

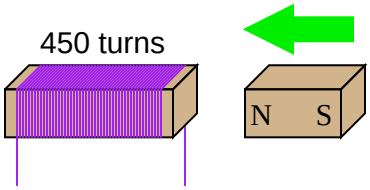


What do you notice about the slope (also called the derivative, or $\frac{dB}{dH}$) of each plot?

file 03515

Question 79

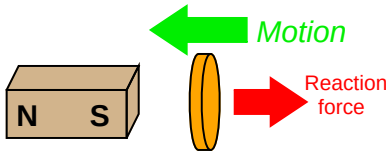
If a wire coil with 450 turns is exposed to a magnetic flux increasing at a rate of 0.008 Webers per second, how much voltage will be induced across the coil?



file 01983

Question 80

Lenz's Law describes the opposition to changes in magnetic flux resulting from electromagnetic induction between a magnetic field and an electrical conductor. One apparatus capable of demonstrating Lenz's Law is a copper or aluminum disk (electrically conductive, but non-magnetic) positioned close to the end of a powerful permanent magnet. There is no attraction or repulsion between the disk and magnet when there is no motion, but a force will develop between the two objects if either is suddenly moved. This force will be in such a direction that it tries to resist the motion (i.e. the force tries to maintain the gap constant between the two objects):



We know this force is magnetic in nature. That is, the induced current causes the disk itself to *become* a magnet in order to react against the permanent magnet's field and produce the opposing force. For each of the following scenarios, label the disk's induced magnetic poles (North and South) as it reacts to the motion imposed by an outside force:

Figure 1

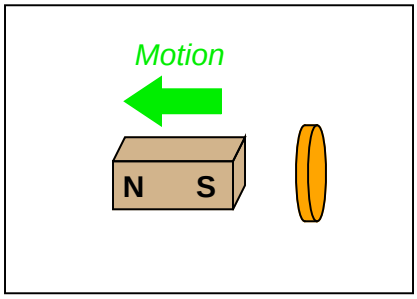


Figure 2

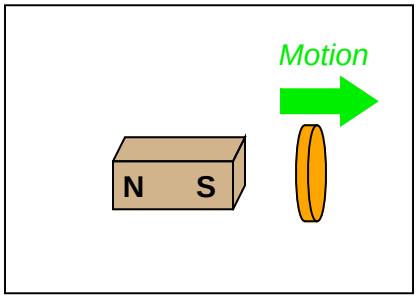


Figure 3

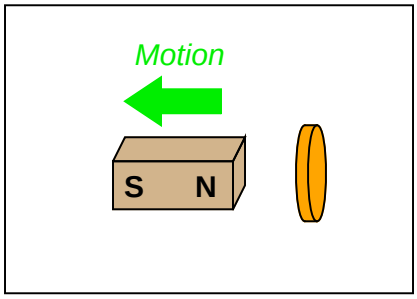
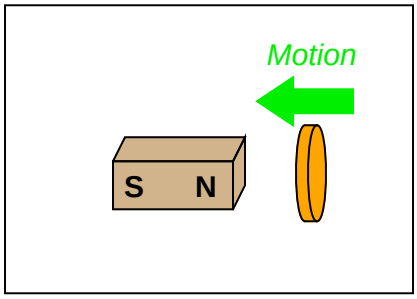


Figure 4



file 01982

Question 81

Combining Lenz's Law with the right-hand rule (or left-hand rule, if you follow electron flow instead of conventional flow) provides a simple and effective means for determining the direction of induced current in an induction coil. In the following examples, trace the direction of current through the load resistor:

Figure 1

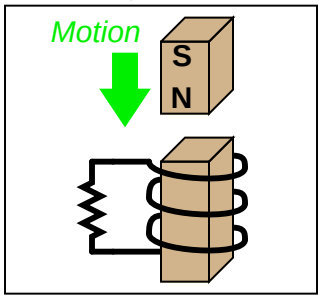


Figure 2

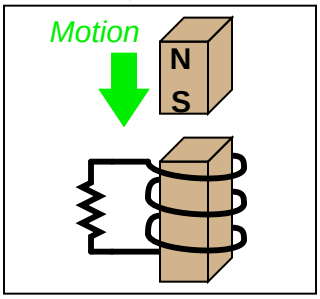


Figure 3

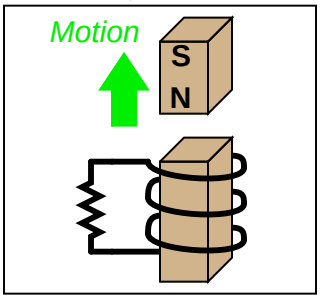


Figure 4

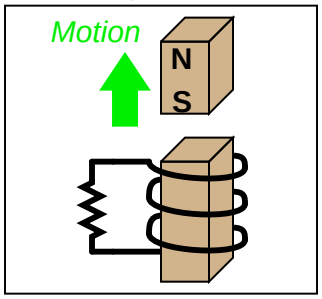


Figure 5

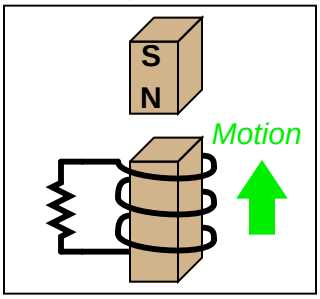
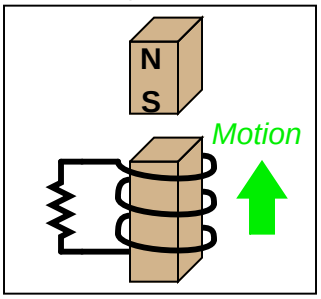


Figure 6

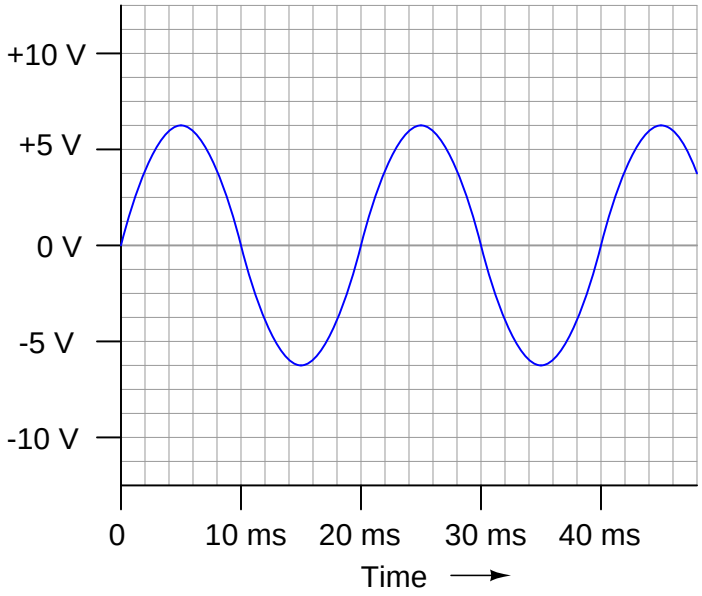


file 01787

Question 82

Apply the following terms to this graph of an AC voltage measured over time:

- Frequency
- Period
- Hertz
- Amplitude



file 00054

Question 83

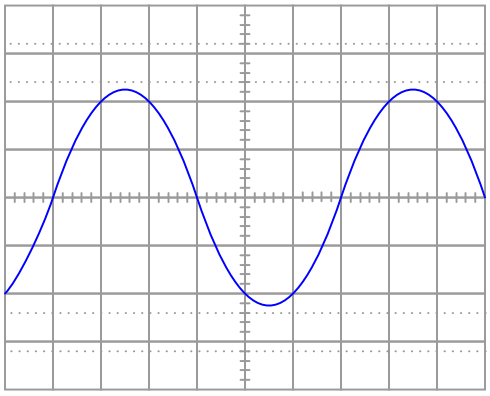
Radio waves are comprised of oscillating electric and magnetic fields, which radiate away from sources of high-frequency AC at (nearly) the speed of light. An important measure of a radio wave is its *wavelength*, defined as the distance the wave travels in one complete cycle.

Suppose a radio transmitter operates at a fixed frequency of 950 kHz. Calculate the approximate wavelength (λ) of the radio waves emanating from the transmitter tower, in the metric distance unit of meters. Also, write the equation you used to solve for λ.

file 01819

Question 84

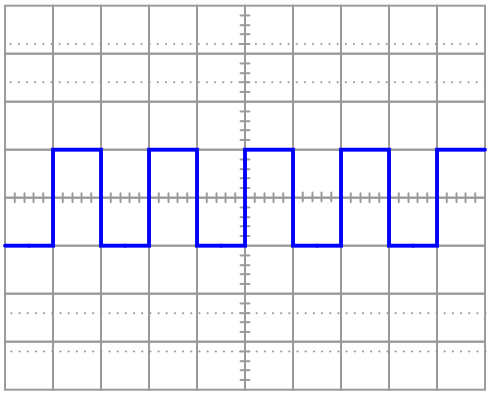
Determine the RMS amplitude of this sinusoidal waveform, as displayed by an oscilloscope with a vertical sensitivity of 0.2 volts per division:



file 01818

Question 85

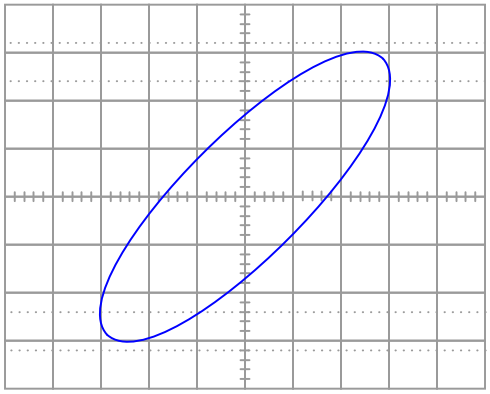
Determine the RMS amplitude of this square-wave signal, as displayed by an oscilloscope with a vertical sensitivity of 0.5 volts per division:



file 01824

Question 86

Calculate the amount of phase shift indicated by this Lissajous figure:



file 03577

Question 87

Read the following quotation, and then research the term **microcontroller** to see what relevance it has to the quote:

I went to my first computer conference at the New York Hilton about 20 years ago. When somebody there predicted the market for microprocessors would eventually be in the millions, someone else said, "Where are they all going to go? It's not like you need a computer in every doorknob!"

Years later, I went back to the same hotel. I noticed the room keys had been replaced by electronic cards you slide into slots in the doors.

There was a computer in every doorknob.

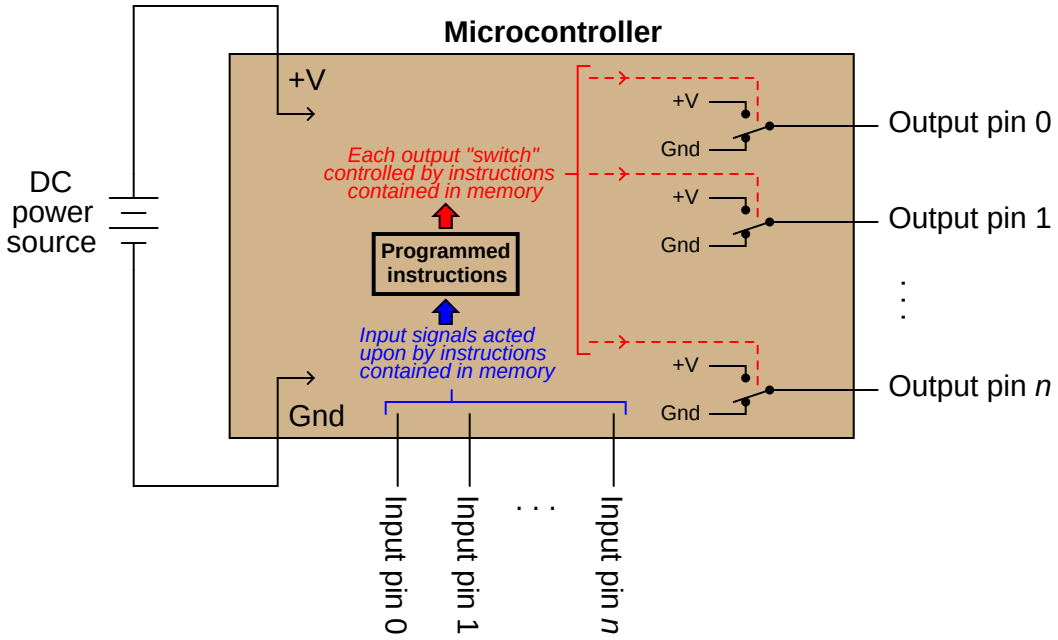
– Danny Hillis

file 02581

Question 88

A *microcontroller unit*, or *MCU*, is a specialized type of digital computer used to provide automatic sequencing or control of a system. Microcontrollers differ from ordinary digital computers in being very small (typically a single integrated circuit chip), with several dedicated pins for input and/or output of digital signals, and limited memory. Instructions programmed into the microcontroller's memory tell it how to react to input conditions, and what types of signals to send to the outputs.

The simplest type of signal "understood" by a microcontroller is a discrete voltage level: either "high" (approximately +V) or "low" (approximately ground potential) measured at a specified pin on the chip. Transistors internal to the microcontroller produce these "high" and "low" signals at the output pins, their actions being modeled by SPDT switches for simplicity's sake:



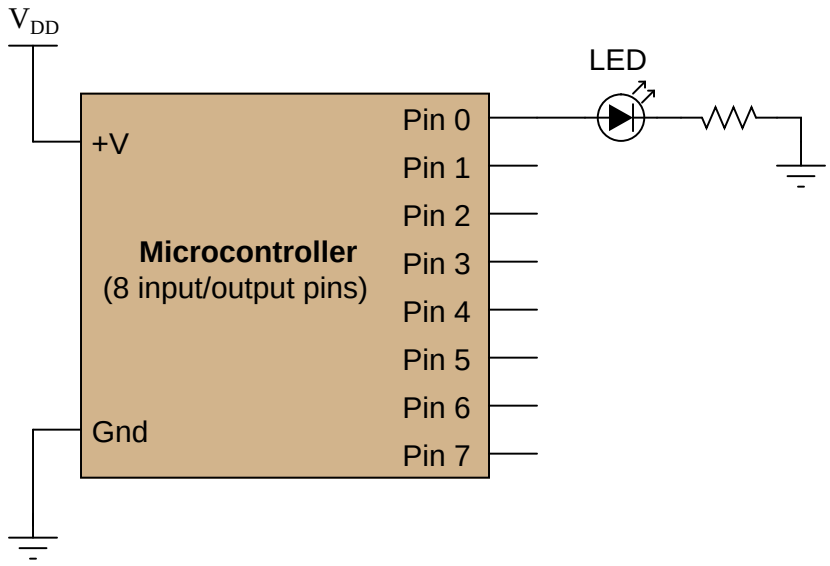
Microcontrollers may be programmed to emulate the functions of digital logic gates (AND, OR, NAND, NOR, etc.) in addition to a wide variety of combinational and multivibrator functions. The only real limits to what a microcontroller can do are memory (how large of a program may be stored) and input/output pins on the MCU chip.

However, microcontrollers are themselves made up of many thousands (or millions!) of logic gate circuits. Why would it make sense to use a microcontroller to perform a logic function that a small fraction of its constituent gates could accomplish directly? In other words, why would anyone bother to program a microcontroller to perform a digital function when they could build the logic network they needed out of fewer gate circuits?

file 02596

Question 89

A student decides to build a light-flasher circuit using a microcontroller instead of a 555 timer or some other hard-wired astable circuit. Unfortunately, there is a problem somewhere. When first powered up, the LED lights on for 1 second, then turns off and never turns back on. The only way the LED ever comes back on is if the MCU is reset or its power is cycled off and on:



Pseudocode listing

```
Declare Pin0 as an output
BEGIN
  Set Pin0 HIGH
  Pause for 1 second
  Set Pin0 LOW
END
```

A fellow student, when asked for help, modifies the program listing and re-sends it from the personal computer where it is being edited to the microcontroller, through a programming cable. The program listing now reads as such:

Pseudocode listing

```
Declare Pin0 as an output
LOOP
  Set Pin0 HIGH
  Pause for 1 second
  Set Pin0 LOW
ENDLOOP
```

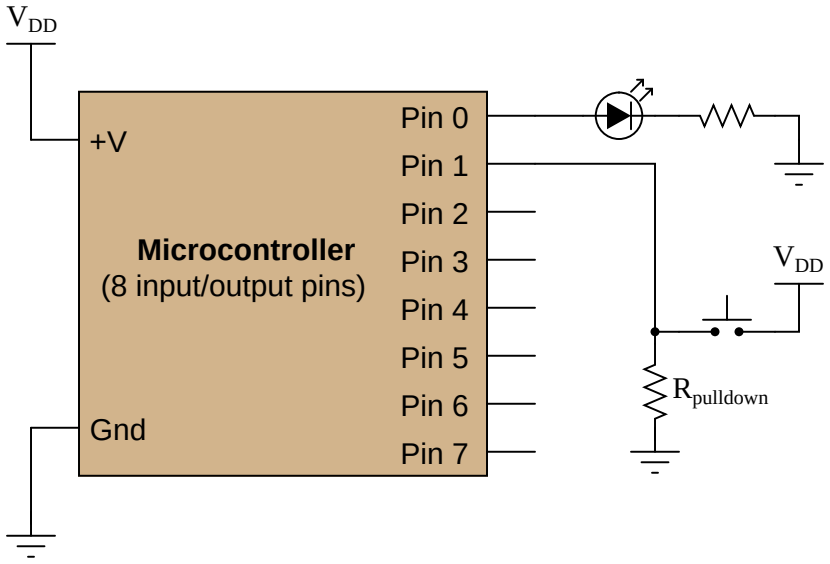
When the MCU is reset with the new program, the LED starts blinking on and off . . . sort of. The LED is "on" most of the time, but once every second it turns off and then immediately comes back on. In fact, the "off" period is so brief it is barely noticeable.

What the student wanted was a 50% duty cycle: "on" for 1 second, then "off" for 1 second, repeating that cycle indefinitely. First, explain the significance of the classmate's program modification, and then modify the program listing again so that the LED does what the student wants it to.

file 02597

Question 90

A student decides to build a light-flasher circuit using a microcontroller. The LED is supposed to blink on and off only when the pushbutton switch is depressed. It is supposed to turn off when the switch is released:



Pseudocode listing

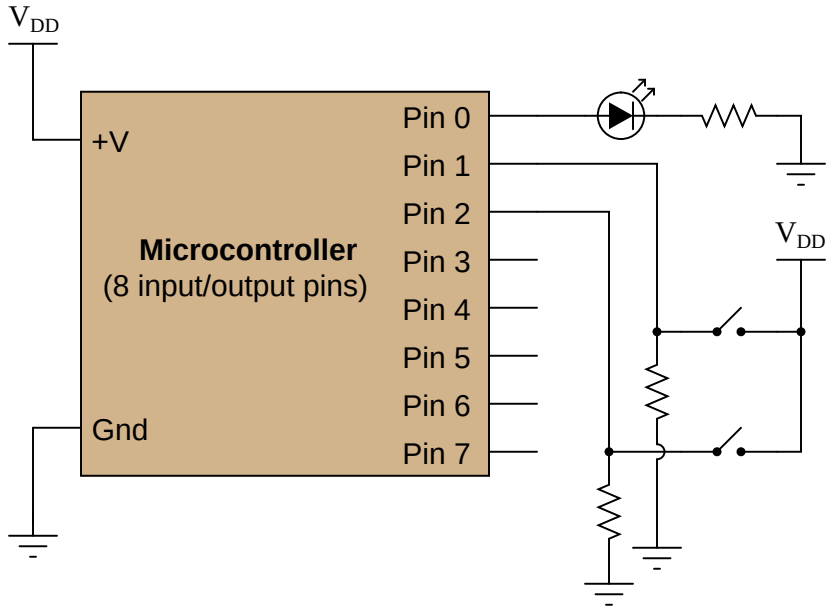
```
Declare Pin0 as an output
Declare Pin1 as an input
WHILE Pin1 is HIGH
  Set Pin0 HIGH
  Pause for 0.5 seconds
  Set Pin0 LOW
  Pause for 0.5 seconds
ENDWHILE
```

The LED blinks on and off just fine as long as the pushbutton switch is held when the MCU is powered up or reset. As soon as the switch is released, the LED turns off and never comes back on. If the switch was never pressed during start-up, the LED never comes on! Explain what is happening, and modify the program as necessary to fix this problem.

file 02598

Question 91

Examine the following schematic diagram and program listing (written in "pseudocode" rather than a formal programming language) to determine what type of basic logic function is being implemented in this microcontroller unit:



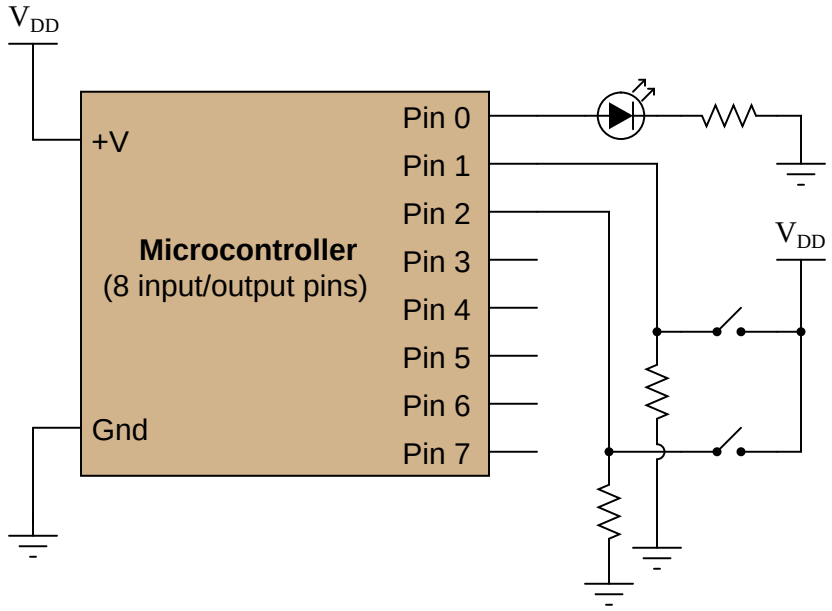
Pseudocode listing

```
Declare Pin0 as an output
Declare Pin1 and Pin2 as inputs
LOOP
  IF Pin1 is HIGH, set Pin0 HIGH
  ELSEIF Pin2 is HIGH, set Pin0 HIGH
  ELSE set Pin0 LOW
  ENDIF
ENDLOOP
```

file 02582

Question 92

Examine the following schematic diagram and program listing (written in "pseudocode" rather than a formal programming language) to determine what type of basic logic function is being implemented in this microcontroller unit:



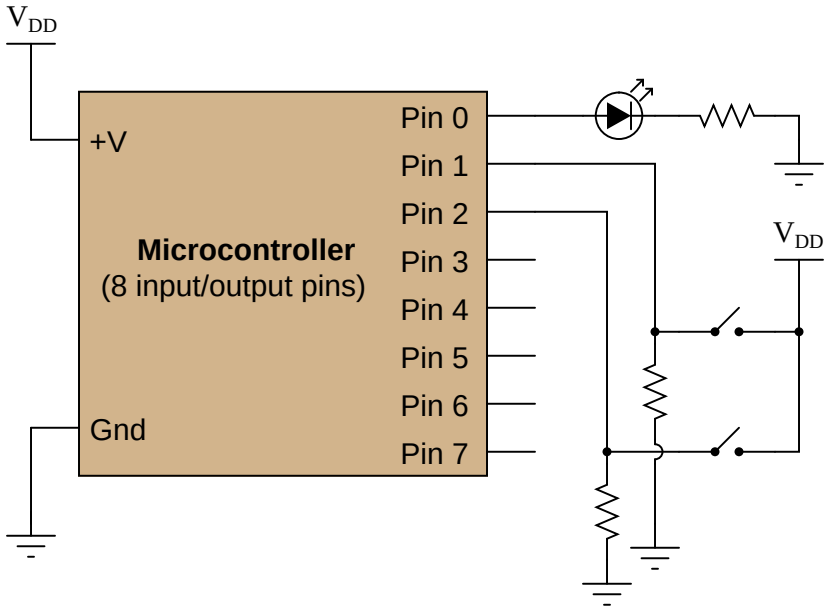
Pseudocode listing

```
Declare Pin0 as an output
Declare Pin1 and Pin2 as inputs
LOOP
  IF Pin1 is LOW, set Pin0 LOW
  ELSEIF Pin2 is LOW, set Pin0 LOW
  ELSE set Pin0 HIGH
  ENDIF
ENDLOOP
```

file 02583

Question 93

Examine the following schematic diagram and program listing (written in "pseudocode" rather than a formal programming language) to determine what type of basic logic function is being implemented in this microcontroller unit:



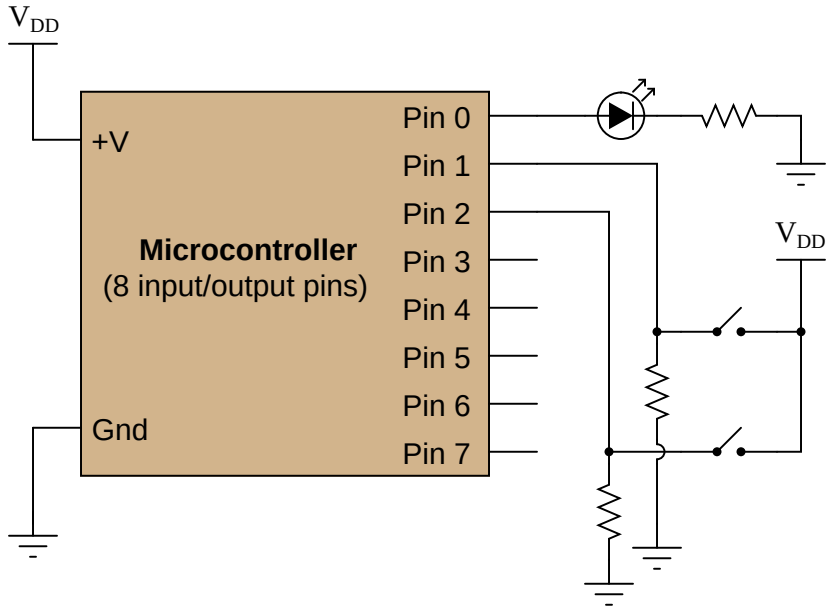
Pseudocode listing

```
Declare Pin0 as an output
Declare Pin1 and Pin2 as inputs
LOOP
  IF Pin1 is LOW, set Pin0 HIGH
  ELSEIF Pin2 is LOW, set Pin0 HIGH
  ELSE set Pin0 LOW
  ENDIF
ENDLOOP
```

file 02584

Question 94

Examine the following schematic diagram and program listing (written in "pseudocode" rather than a formal programming language) to determine what type of basic logic function is being implemented in this microcontroller unit:



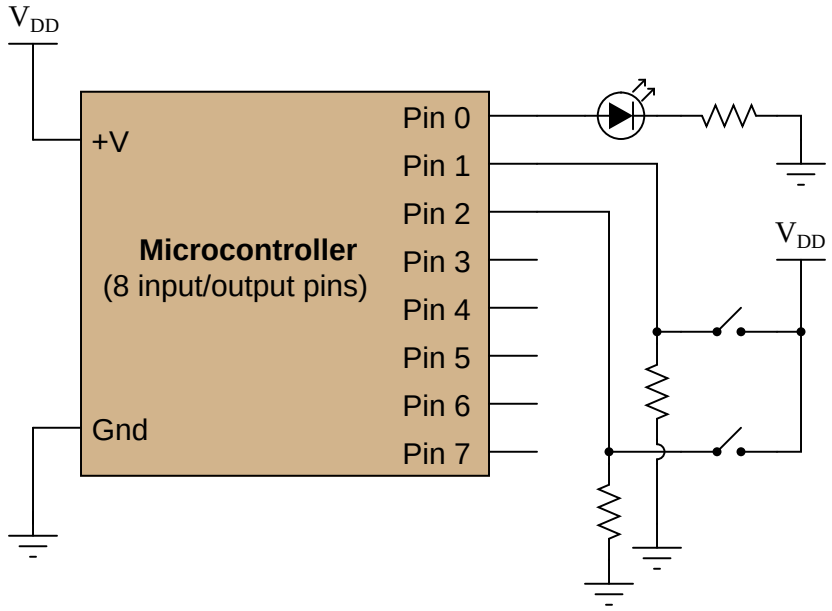
Pseudocode listing

```
Declare Pin0 as an output
Declare Pin1 and Pin2 as inputs
LOOP
  IF Pin1 is HIGH, set Pin0 LOW
  ELSEIF Pin2 is HIGH, set Pin0 LOW
  ELSE set Pin0 HIGH
  ENDIF
ENDLOOP
```

file 02585

Question 95

Examine the following schematic diagram and program listing (written in "pseudocode" rather than a formal programming language) to determine what type of basic logic function is being implemented in this microcontroller unit:



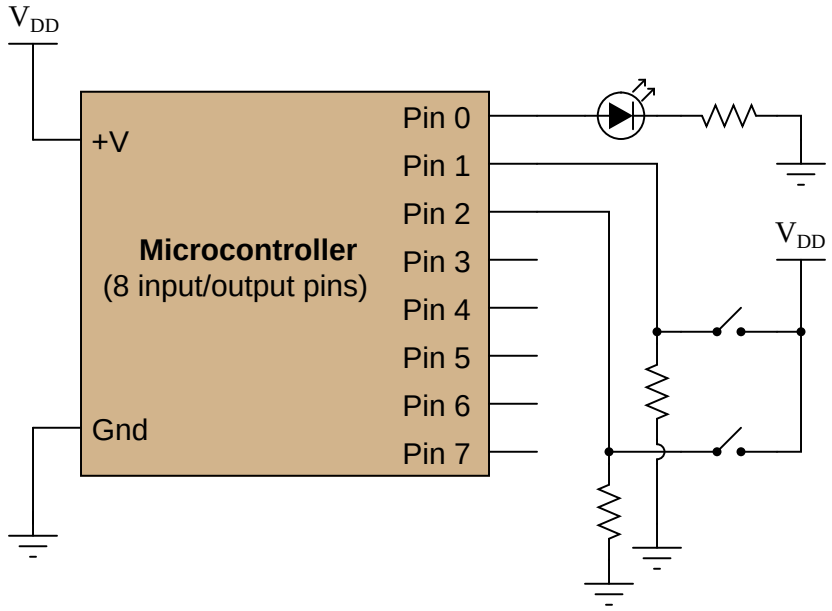
Pseudocode listing

```
Declare Pin0 as an output
Declare Pin1 and Pin2 as inputs
LOOP
  IF Pin1 is same as Pin2, set Pin0 LOW
  ELSE set Pin0 HIGH
  ENDIF
ENDLOOP
```

file 02586

Question 96

Examine the following schematic diagram and program listing (written in "pseudocode" rather than a formal programming language) to determine what type of basic logic function is being implemented in this microcontroller unit:



Pseudocode listing

```
Declare Pin0 as an output
Declare Pin1 and Pin2 as inputs
LOOP
  IF Pin1 is same as Pin2, set Pin0 HIGH
  ELSE set Pin0 LOW
  ENDIF
ENDLOOP
```

file 02587

Question 97

Identify whether each of these quantities is *continuous* or *discrete*:

- Resistance of a rheostat:
- Resistance of a switch:
- Time represented by an analog clock:
- Time represented by a digital clock:
- Quantity of money in a billfold (bills and coins):
- Number of pebbles held in a hand:
- A person's weight, in pounds or kilograms:
- Voltage output by a comparator:
- Voltage output by an operational amplifier:
- Electrical conductivity of a thyristor:

file 02754

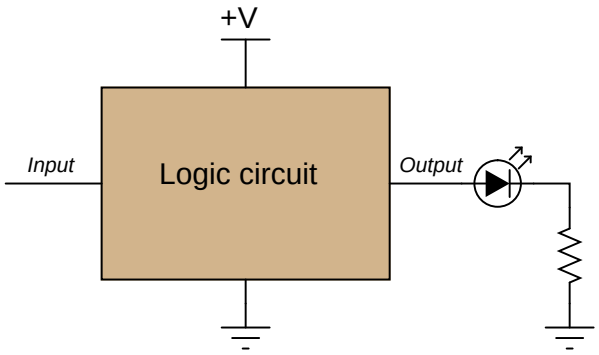
Question 98

Two computational aids of antiquity are the *abacus* and the *slide rule*. Which of these mathematical instruments would be considered "analog" and which would be considered "digital"? Explain your answer.

file 02757

Question 99

In digital electronic circuitry, binary bit values of 0 or 1 are represented in the form of voltages: *low* and *high* logic states, respectively. Suppose you need to manually "input" a logic state to one of the pins of a logic circuit. In the following illustration, the logic circuit (shown as an indistinct, shaded rectangle) is already supplied with DC power (+V and ground), and its output is indicated by an LED. All it requires is an input from you:

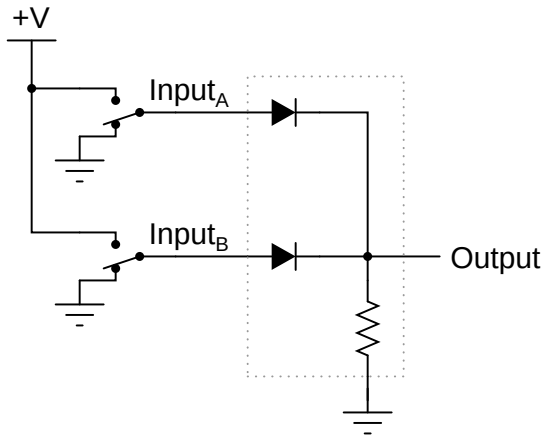


Complete this schematic diagram by including a switch in the drawing, such that in each of its two positions, a definite "low" or "high" logic state will be sensed by the circuit's input terminal.

file 01251

Question 100

Crude logic gates circuits may be constructed out of nothing but diodes and resistors. Take for example this logic gate circuit:



Identify what type of logic function is represented by this gate circuit (AND, OR, inverter, etc.).

file 02763

Question 101

One way to think of the basic logic gate types (all but the XOR and XNOR gates) is to consider what single input state guarantees a certain output state. For example, we could describe the function of an OR gate as such:

Any high input guarantees a high output.

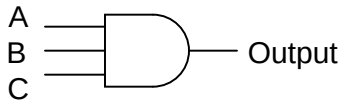
Identify what type of gate is represented by each of the following phrases:

- Any high input guarantees a low output.
- Any low input guarantees a high output.
- Any low input guarantees a low output.

file 02891

Question 102

Complete the truth table for a three-input AND gate:



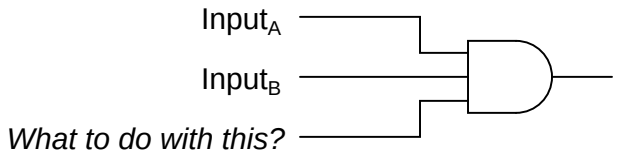
A	B	C	Output
0	0	0	
0	0	1	
0	1	0	
0	1	1	
1	0	0	
1	0	1	
1	1	0	
1	1	1	

file 02915

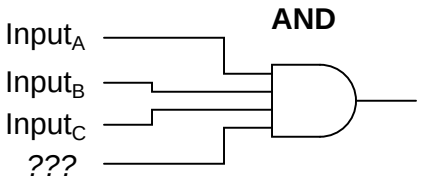
Question 103

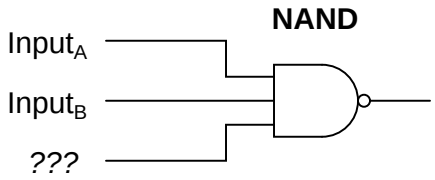
Suppose you needed a two-input AND gate, but happened to have an unused 3-input AND gate in one of the integrated circuits ("chips") already in the system you were building. Of course, you could just add another IC containing 2-input AND gates, but it seems a shame to waste the 3-input gate already there.

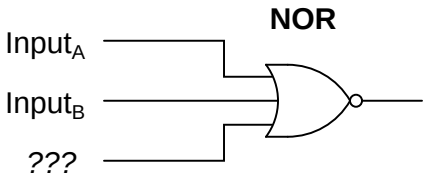
Explain what you would need to do with the third input terminal on this gate in order to use it as a 2-input AND gate:

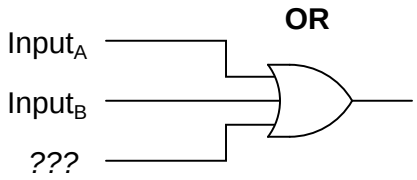


Now, explain what to do with each of the following gates' third inputs, in order to use each of them as 2-input gates:









In each case, describe why your solution works.

file 02948

Question 104

In TTL circuitry, one side of the DC power supply is usually labeled as "V_{CC}", while the other side is labeled as "V_{EE}". Why is this? What do the subscripts "CC" and "EE" represent?

file 01263

Question 105

True story: once upon a time, there was a machine shop containing a number of computer-controlled machine tools (lathes, mills, grinders, etc.), where one of the machines proved to be very "finicky" when starting. Sometimes, it would function properly when you pushed the "Start" button, and other times it refused to work at all. The problem was so bad, it got to the point where the machinists responsible for operating this tool became almost superstitious about it, performing a ritual dance before pressing the "Start" button, whimsically hoping to improve their luck.

An electrician was called to service this machine, but he could find nothing wrong with the electrical power circuitry. All of the high-voltage equipment (transformers, relays, motors, motor control circuits, etc.) seemed to be in good working order. The problem, whatever it was, resided within the machine's electronic control computer. The computer was not sending the "start" signal to the motor control circuits when the "Start" button was pushed.

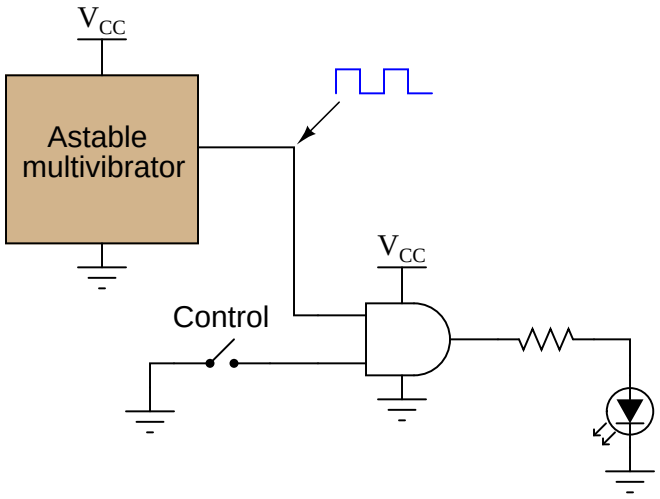
An electronics technician was called to troubleshoot the computer, and he was able to fix it in a matter of minutes. The problem, he said, was the computer's DC power supply: the voltage regulator was out of adjustment. With just a twist of a potentiometer, the technician was able to "trim" the regulated voltage to 5.00 volts, right where it should be for TTL circuitry.

The power supply voltage was not very far from 5.00 volts before the technician adjusted it. How far is the supply voltage allowed to deviate for TTL logic circuits, and still have guaranteed proper operation? Consult one or more IC datasheets for legacy TTL logic circuits (not the newer high-speed CMOS 54HCxx and 74HCxx chips) to obtain your answer.

file 01261

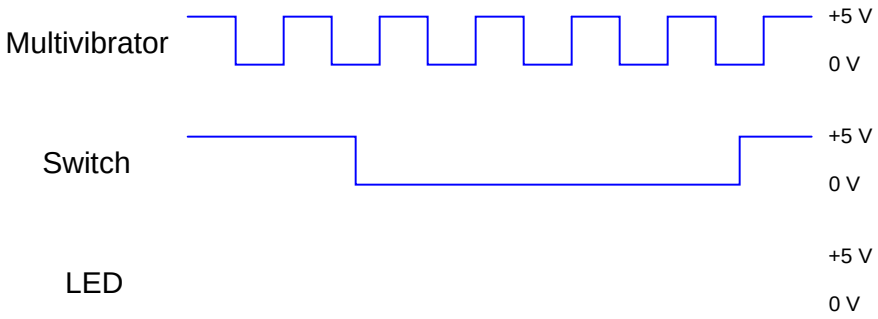
Question 106

In this circuit, an AND gate is used to give a toggle switch control over the blinking of an LED:



The "astable multivibrator" is nothing more than an oscillator that produces a square-wave signal at a low frequency, at standard TTL voltage levels (0 and +5 volts).

Plot the output waveform for the gate (i.e. the voltage signal to the LED), given the following input conditions:

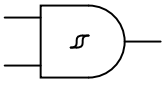


Hint: it helps in your analysis of digital waveforms if you first write a truth table for the gate under consideration, for your reference.

file 01345

Question 107

What does it mean if you see a logic gate symbol in a schematic diagram with a strange-looking "S" figure drawn inside of it?



file 01281

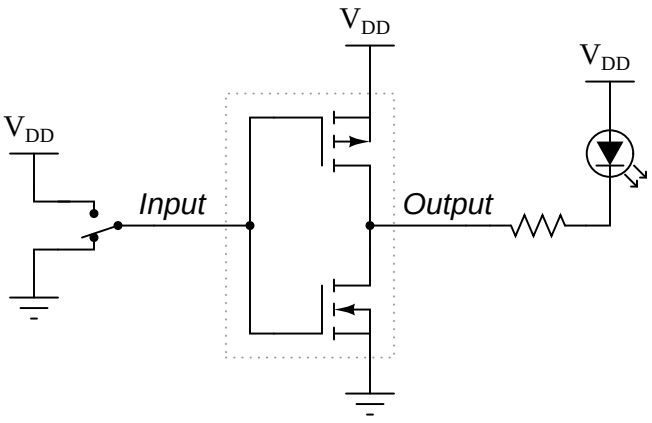
Question 108

In CMOS circuitry, one side of the DC power supply is usually labeled as "V_{DD}", while the other side is labeled as "V_{SS}". Why is this? What do the subscripts "DD" and "SS" represent?

file 01273

Question 109

A very important concept to understand in digital circuitry is the difference between *current sourcing* and *current sinking*. For instance, examine this CMOS inverting buffer gate circuit, connected to a load:

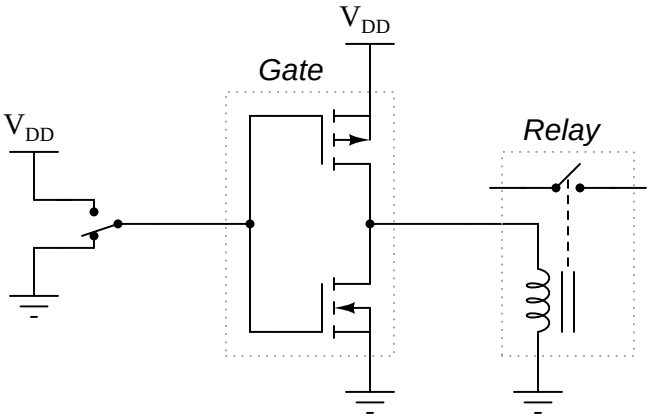


Is this gate circuit configured to *source* load current, *sink* load current, or do both?

file 01259

Question 110

Suppose that a CMOS inverting buffer gate were to drive a predominantly inductive load, such as a small relay coil:



Normally, it would be considered good design practice to connect a commutating diode in parallel with the relay coil, to prevent high-voltage transients when the coil is de-energized. However, this is not necessary when a CMOS gate drives a coil. Explain why.

file 01271

Question 111

A problem unique to certain types of CMOS logic gates is something called *SCR latchup*. This is an abnormal condition capable of ruining a circuit, or at the very least causing operational problems in a circuit. Explain what this phenomenon is, and what causes it.

file 01248

Question 112

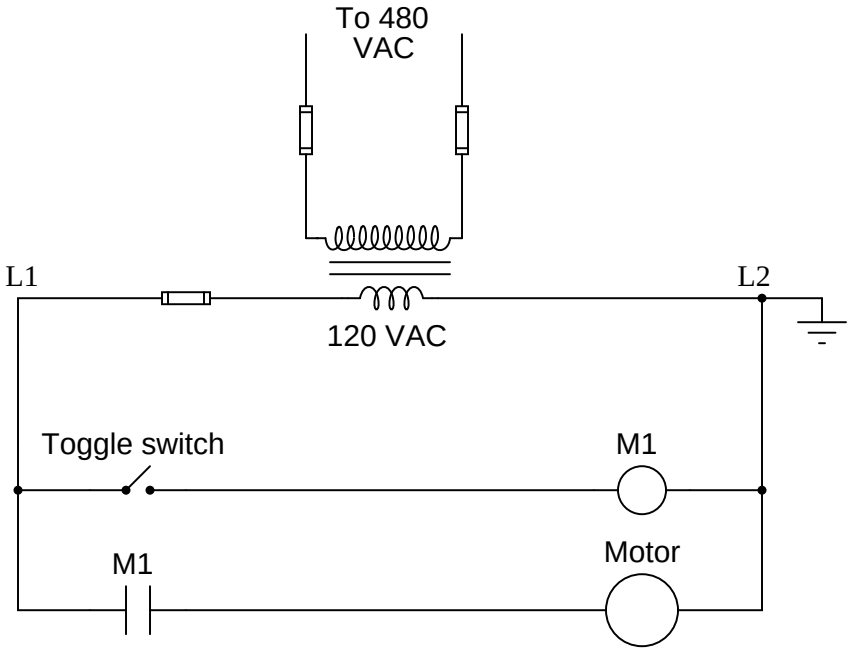
Explain why placing static-sensitive components (such as CMOS integrated circuits) into a block of conductive foam protects them against damage from ESD, and why this protection exists even if the entire block of foam (with chip) is brought to an elevated potential with respect to earth ground.

file 02869

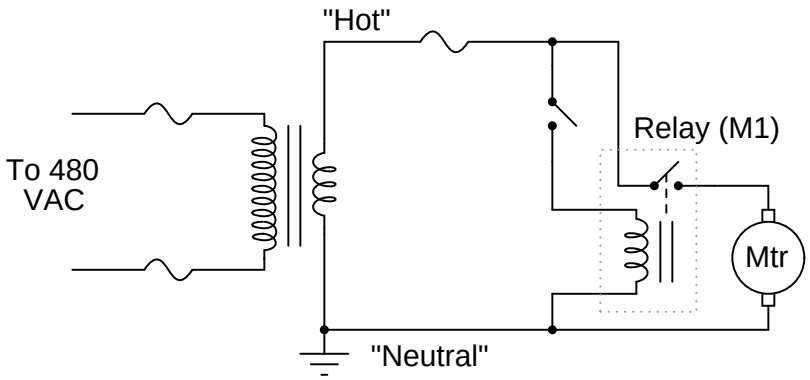
Question 113

Perhaps the most challenging aspect of interpreting ladder diagrams, for people more familiar with electronic schematic diagrams, is how electromechanical relays are represented. Compare these two equivalent diagrams:

First, the ladder diagram:



Next, the schematic diagram:

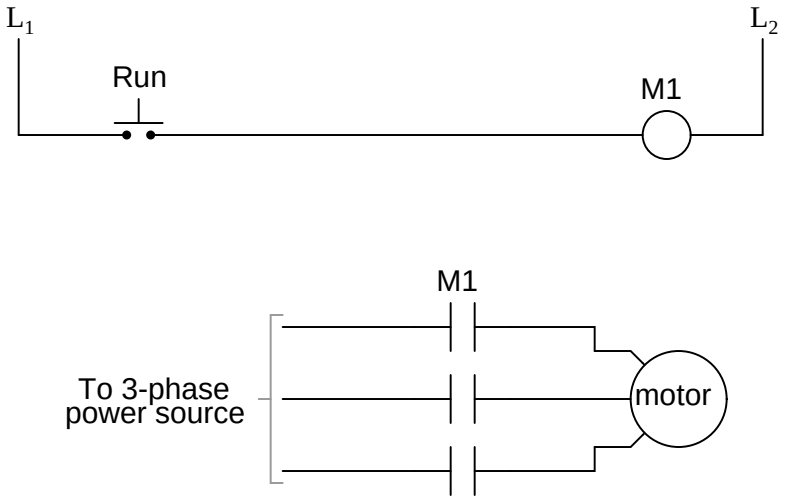


Based on your observations of these two diagrams, explain how electromechanical relays are represented differently between ladder and schematic diagrams.

file 00833

Question 114

Interpret this AC motor control circuit diagram, explaining the meaning of each symbol:

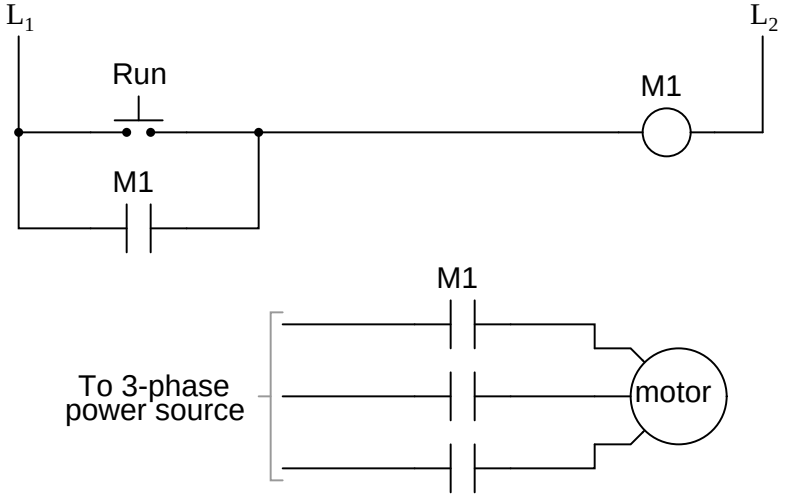


Also, explain the operation of this motor control circuit. What happens when someone actuates the "Run" switch? What happens when they let go of the "Run" switch?

file 00834

Question 115

Interpret this AC motor control circuit diagram, explaining the meaning of each symbol:



Also, explain the operation of this motor control circuit. What happens when someone actuates the "Run" switch? What happens when they let go of the "Run" switch?

file 00835

Question 116

Suppose you come across a relay that is said to have "Form C" contacts. What does this phrase mean? And, is there such a thing as either "Form A" or "Form B" contacts?

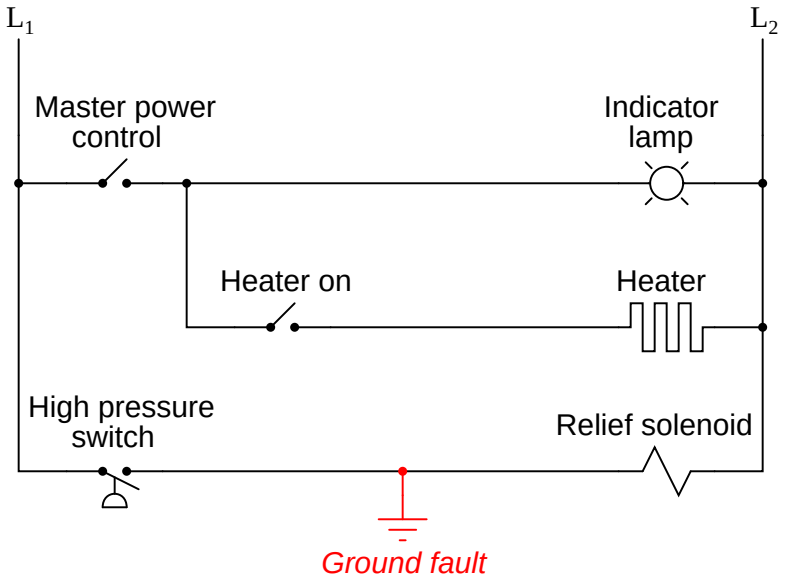
file 01387

Question 117

Safety is a paramount concern in electrical systems. Generally, we try to design electrical circuits so that if and when they fail, they will do so in the manner safest to those people working around them, and to the equipment and process(es) controlled by the circuit.

One of the more common failure modes of circuits having wires strung through metal conduit is the *accidental ground*, or *ground fault*, where the electrical insulation surrounding a wire fails, resulting in contact between that wire and a grounded metal surface.

Suppose an accidental ground were to occur at the point shown in this ladder diagram:



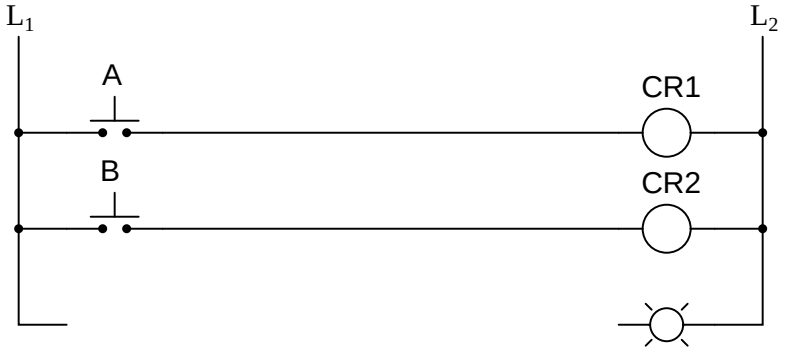
What would be the result of this fault? Hint: you will need to know something about the L1/L2 power source in order to answer this question!

What would be the result if the L1/L2 power connections were reversed?

file 01291

Question 118

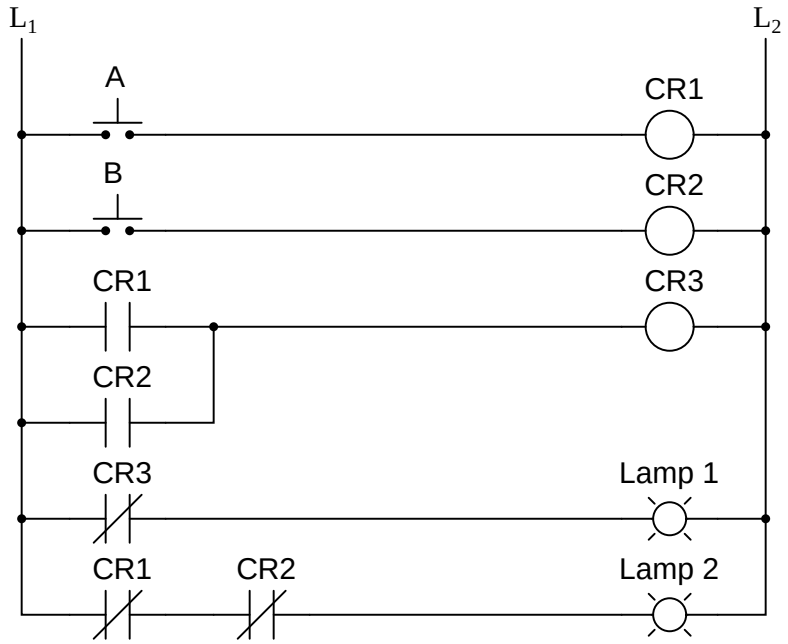
Complete the following ladder logic diagram so that an AND gate function is formed: the indicator lamp energizes if and only if both switch A *and* switch B are simultaneously actuated.



file 01292

Question 119

Write a truth table for each of the indicator lamps in the following ladder diagram, and determine which logic function (AND, OR, NAND, NOR, or NOT) best describes each lamp's behavior with respect to the status of the input switches.



file 01294

Answers

Answer 1

A *continuous* quantity is one that may be smoothly varied from one extreme value to another, while a *discrete* quantity is one that can only assume a finite (limited) number of distinct states. Here, the rheostat exhibits a *continuously* adjustable electrical continuity while the switch is *discrete* because it can only be conducting or non-conducting.

Follow-up question: what is the difference between a continuous voltage versus a discrete voltage?

Answer 2

"High" = (nearly) 5 volts between the gate input/output and ground.

"Low" = (nearly) 0 volts between the gate input/output and ground.

Answer 3

- V_{TP1} = *high*
- V_{TP2} = *high*
- V_{TP3} = *low*
- V_{TP4} = *high*
- Transistor = *off*
- LED = *off*

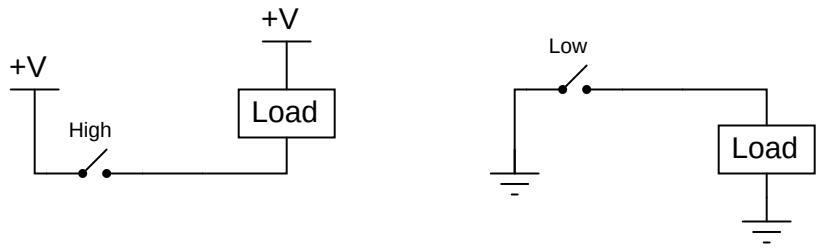
Follow-up question: show how you would calculate reasonable values for the two resistors in this circuit.

Answer 4

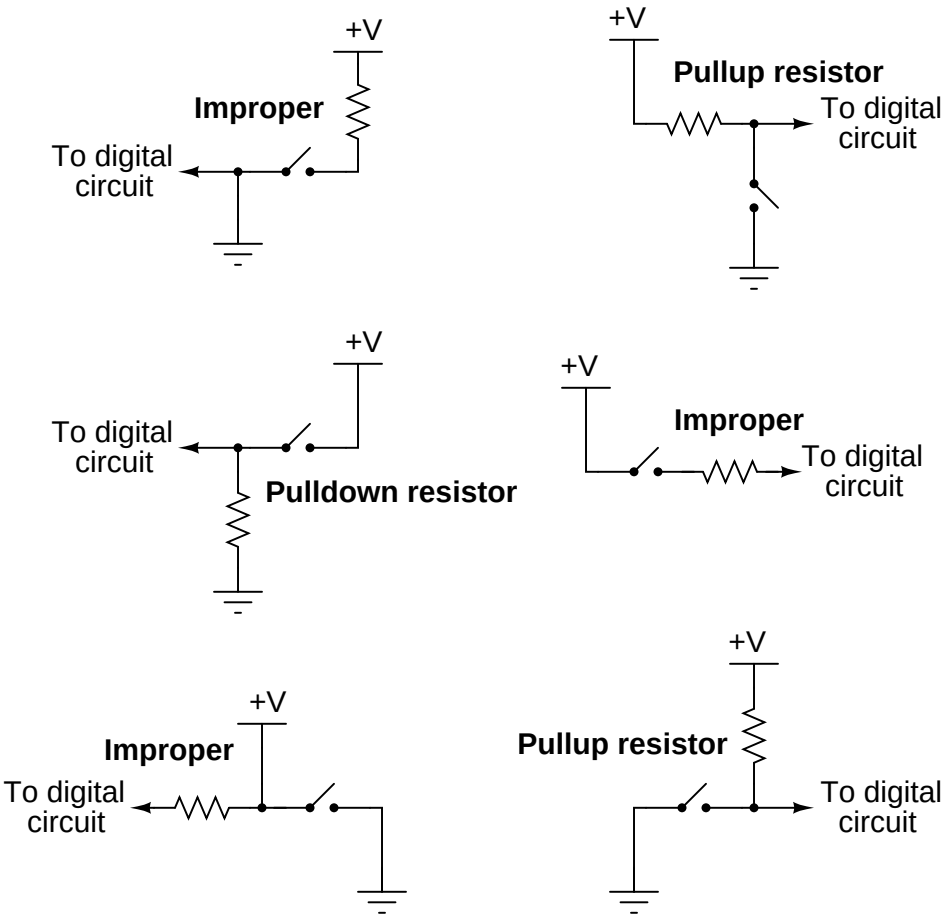
The "pulldown" and "pullup" resistors do exactly what their names imply: they *pull* the logic state of the wire in the direction opposite what the switch does when closed.

Follow-up question: to better understand the purpose of these resistors, examine the following circuits without pulldown and pullup resistors to determine what the logic states of the wires will be in both switch positions. Then, add either pulldown or pullup resistors and re-examine the circuits:

Challenge question: how does one calculate the proper resistance (in ohms) for a pulldown or pullup resistor? Will any size work, or is there such a thing as too large or too small?



Answer 5



Follow-up question: specifically identify what would be wrong with each of the "improper" circuits.

Answer 6

I'll let you and your classmates figure out how this circuit functions!

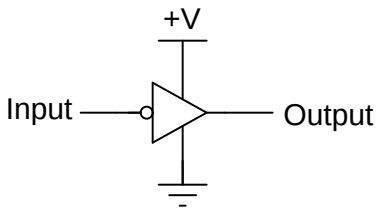
Follow-up question #1: explain how you could use a voltmeter as a logic probe to do troubleshooting in a digital circuit.

Follow-up question #2: write a formula for calculating appropriate current-limiting resistor sizes for the two LEDs in this circuit, given the value of $+V$ and the LED forward voltage and current values.

Answer 7

This is an **inverter** gate, so named because its output is always the opposite (inverted) state as the input.

Note: inverter gates are often shown like this instead:



Note: inverter gates are sometimes referred to as **NOT** gates, because when the input is high, the output will *not* be high.

Answer 8

This is an **AND** gate, so named because its output goes high only if input A is high *and* input B is high.

Follow-up question: show how a light-emitting diode could be connected to the output of this logic gate to provide visual indication of its output state.

Challenge question: show how this logic gate could drive a high-current load such as a solenoid or an electric motor.

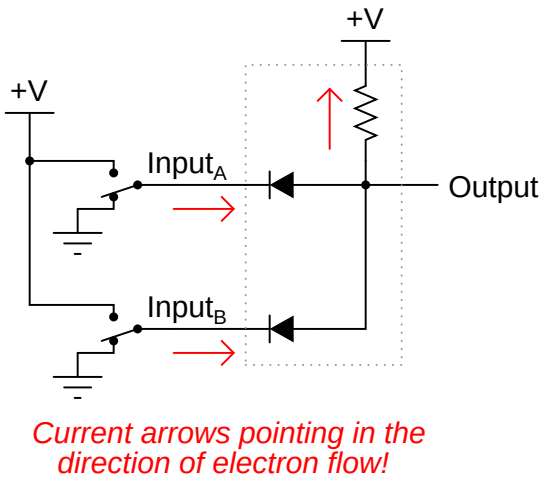
Answer 9

This is an **OR** gate, so named because its output goes high if either input A is high *or* input B is high.

Follow-up question: replace the two SPDT switches with SPST switches, complete with pullup or pulldown resistors as necessary.

Answer 10

This is an AND gate circuit.

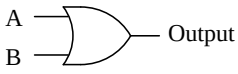


Follow-up question: show how the two SPDT switches could be replaced by SPST switches (without the need for pullup or pulldown resistors).

Challenge question: explain why it may be impractical to design this diode-resistor gate circuit to directly drive an LED so that it lights up when the output state is "high."

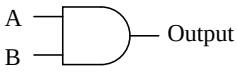
Answer 11

OR



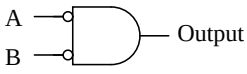
A	B	Output
0	0	0
0	1	1
1	0	1
1	1	1

AND



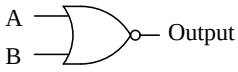
A	B	Output
0	0	0
0	1	0
1	0	0
1	1	1

Neg-AND



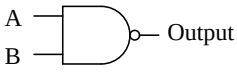
A	B	Output
0	0	1
0	1	0
1	0	0
1	1	0

NOR



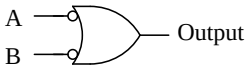
A	B	Output
0	0	1
0	1	0
1	0	0
1	1	0

NAND



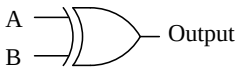
A	B	Output
0	0	1
0	1	1
1	0	1
1	1	0

Neg-OR



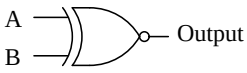
A	B	Output
0	0	1
0	1	1
1	0	1
1	1	0

XOR



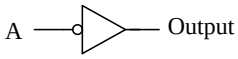
A	B	Output
0	0	0
0	1	1
1	0	1
1	1	0

XNOR



A	B	Output
0	0	1
0	1	0
1	0	0
1	1	1

NOT



A	Output
0	1
1	0

Answer 12

Input	Output
Low	High
High	Low

Answer 13

This is a NAND gate circuit.

Answer 14

TTL gates equipped with totem-pole output circuitry are able to both *source* and *sink* load current. In this particular case, the way the load (LED) is connected to the output of the gate, the gate will only *source* current. However, the gate is capable of sinking current from a load, if only the load were connected differently.

Follow-up question: does the input device driving this TTL gate circuit (the switch in this particular example) have to *source* current, *sink* current, or both?

Challenge question: explain how you would calculate the current sourcing and current sinking abilities of this logic gate circuit, if you were given the internal component values and parameters.

Answer 15

Open-collector gate circuits are only able to *sink* load current. They cannot "source" any load current at all.

Follow-up question #1: what would need to be added to the gate circuit shown, in order for it to have the ability to source load current as well as sink load current?

Follow-up question #2: explain how you would calculate current sinking ability of this logic gate circuit, if you were given the internal component values and parameters.

Answer 16

TTL input devices must be *current-sinking*: that is, they must *ground* the TTL gate input in one of their states. I'll let you figure out why this is so, from the schematic diagrams of TTL logic gate circuits.

Answer 17

I'll let you do your own research on this question. DO NOT obtain your answer from a textbook, but consult a manufacturer's datasheet instead!

Follow-up question: given the standard V_{CC} voltage level of 5.0 volts for TTL circuits, and assuming the use of LEDs that drop 1.7 volts at 20 mA, calculate an appropriate resistance value for the two LED current-limiting resistors.

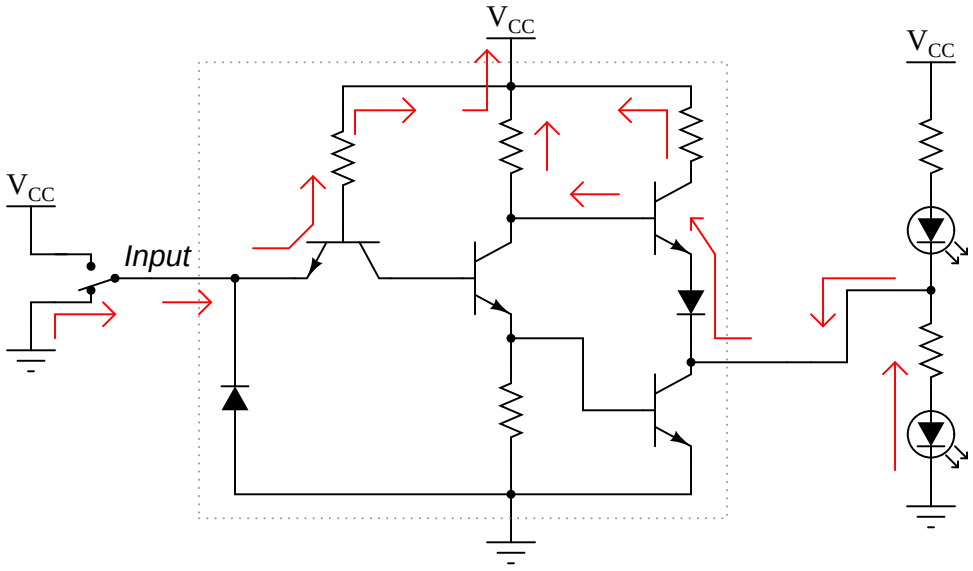
Challenge question: the logic probe circuit shown is minimal in component count. To make a more practical and reliable probe, one would probably want to have reverse-polarity protection (in case someone were to accidently connect the probe backward across the power supply) as well as decoupling for immunity against electrical noise. Add whatever necessary components you think there should be in this circuit to provide these features.

Answer 18

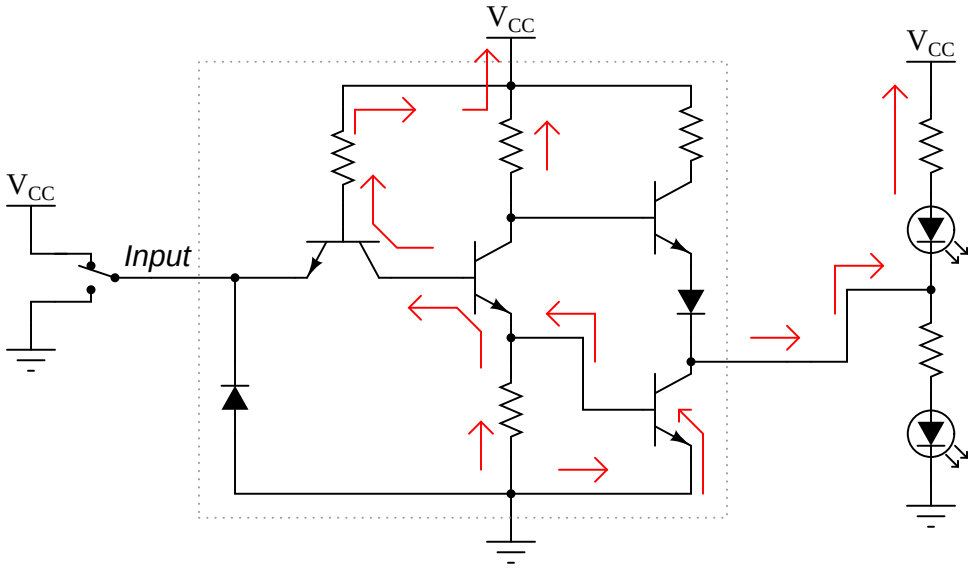
To use a multimeter as a logic probe, connect the common (black) test lead to the power supply ground, set the meter to measure DC voltage (a 0-5 volt scale would be perfect in this application), and then use the other test lead (red) to probe the various points of the circuit.

The problem with this student's circuit is the input switch: it does not provide a solid "low" state when open. Rather, the inverter's input is left "floating" when the switch is unactuated. There is more than one way to fix this design flaw, but I'll leave the details up to you!

Answer 19



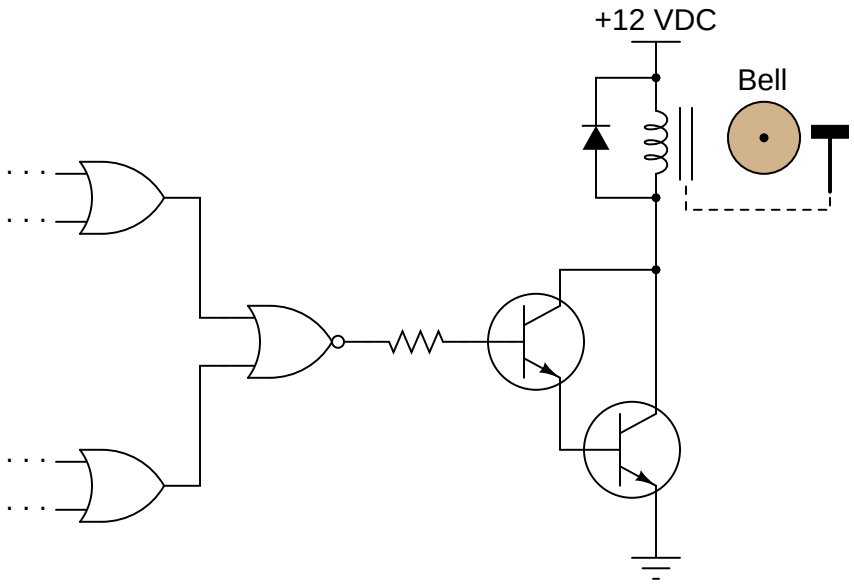
All arrows pointing in the direction of electron flow!



All arrows pointing in the direction of electron flow!

In each scenario, the LED's power is supplied by V_{CC} and ground: the DC power source. Note that the input switch merely "tells" the output what to do rather than handle actual load current, just like the inputs of an operational amplifier or comparator.

Answer 20

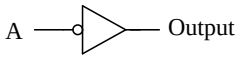


Follow-up question: explain why pullup resistors are not required in this circuit.

Challenge question: sometimes engineers and technicians alike overlook the most elegant (beautifully simple) solutions in their quest to solve a problem. The solution shown here, while practical, solves the problem by adding components to the circuit. Can you think of a way we might build a unanimous-yea vote detector using *fewer* components than the original LED circuit?

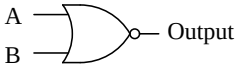
Answer 21

NOT



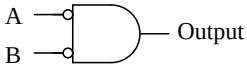
A	Output
0	1
1	0

NOR



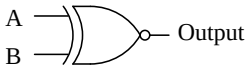
A	B	Output
0	0	1
0	1	0
1	0	0
1	1	0

Neg-AND



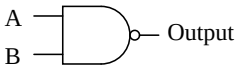
A	B	Output
0	0	1
0	1	0
1	0	0
1	1	0

XNOR



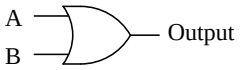
A	B	Output
0	0	1
0	1	0
1	0	0
1	1	1

NAND



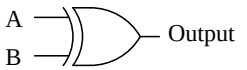
A	B	Output
0	0	1
0	1	1
1	0	1
1	1	0

OR



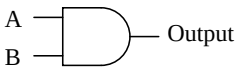
A	B	Output
0	0	0
0	1	1
1	0	1
1	1	1

XOR



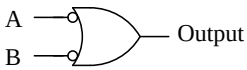
A	B	Output
0	0	0
0	1	1
1	0	1
1	1	0

AND



A	B	Output
0	0	0
0	1	0
1	0	0
1	1	1

Neg-OR



A	B	Output
0	0	1
0	1	1
1	0	1
1	1	0

Answer 22

Input	Output
Low	High
High	Low

Answer 23

Two of the diodes protect against input voltages exceeding the supply rails, while the third diode protects against a reverse-connected power supply.

Answer 24

The resistor on the input side of the gate functions as a *pulldown*, to provide a solid "low" state to the gate's input when the switch contacts open.

Shorting all unused gate inputs to either ground or V_{DD} is merely a precautionary measure. It prevents unnecessary power draw from the supply, and possible IC overheating.

Answer 25

This is a NOR gate.

Follow-up question: identify a series of "thought experiments" you could perform on this circuit schematic to determine the identity of the gate. In other words, document what imagined conditions you would subject this gate to, and what the resulting output states would signify, in answering the question of what type of gate this is.

Answer 26

3 to 18 VDC is typical, though some integrated circuits may have slightly different ratings.

Answer 27

I'll let you do your own research on this question. DO NOT obtain your answer from a textbook, but consult a manufacturer's datasheet instead! You will find that the acceptable voltage levels vary with the power supply voltage, but that the *percentages* are rather constant.

Follow-up question: write a formula for calculating appropriate current-limiting resistor sizes for the two LEDs in this circuit, given the value of $+V$ and the LED forward voltage and current values.

Challenge question: the logic probe circuit shown is minimal in component count. To make a more practical and reliable probe, one would probably want to have reverse-polarity protection (in case someone were to accidently connect the probe backward across the power supply) as well as decoupling for immunity against electrical noise. Add whatever necessary components you think there should be in this circuit to provide these features.

Answer 28

The most obvious problem with this door lock system is the small number of possible codes. It would be rather easy (especially for someone adept at counting in binary!) to simply try all the possible combinations until they gained access.

Here is what I recommend as a strategy for improving the level of security offered by this system: install a fifth pushbutton switch as an "Enter" key. If someone enters the correct four-bit code and then pushes the "Enter" button, the door will open. However, if someone enters the wrong four-bit code and pushes the "Enter" button, the door will not open and a loud alarm will sound! This makes it "risky" to enter a wrong code, thus improving the security of the system.

Follow-up question: modify the circuit shown to implement an improved measure of security – either the strategy suggested or one of your own design.

Answer 29

Buffered gates exhibit better noise immunity than unbuffered gates. One disadvantage to buffering, though, is increased propagation delay time.

Follow-up question: identify the on/off states of all transistors in the buffered circuit for both (high and low) input conditions.

Answer 30

I'll let you research the answer to this question!

Answer 31

Like semiconductor gates, electromechanical relays have but two states: energized and de-energized (1 and 0). Like gates, the contacts of relays may be interconnected to perform standard logic functions such as AND, OR, NAND, NOR, and NOT.

Answer 32

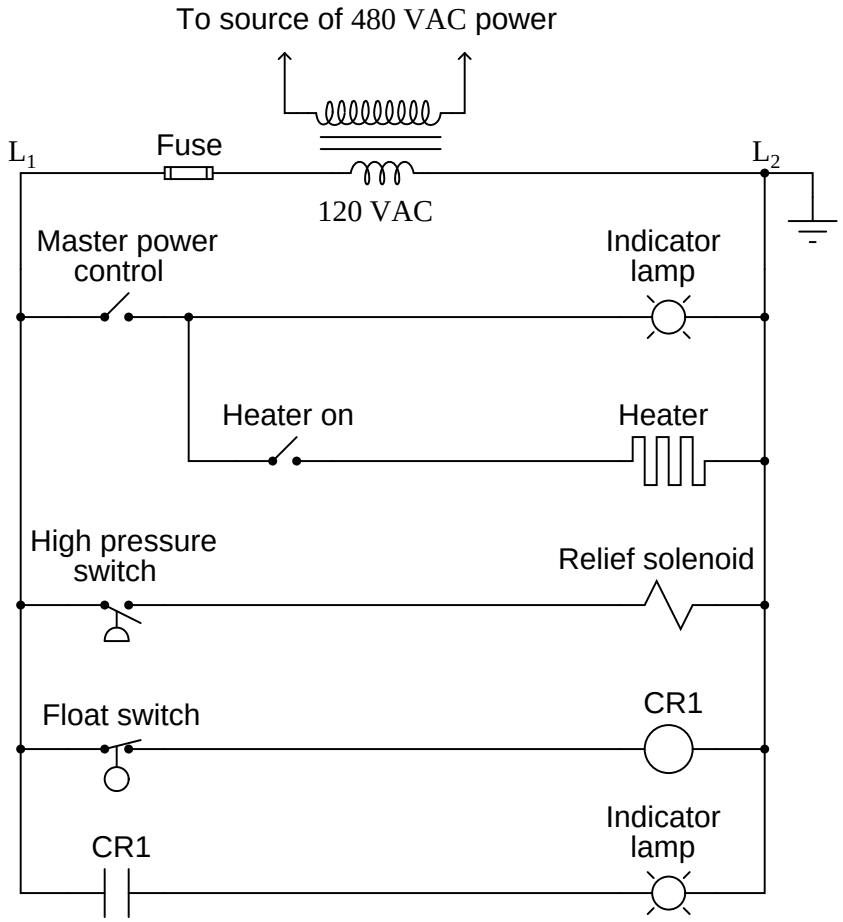
This is an AND function.

Answer 33

This is an OR function.

Answer 34

This is just one example of how the ladder logic diagram could be expanded:

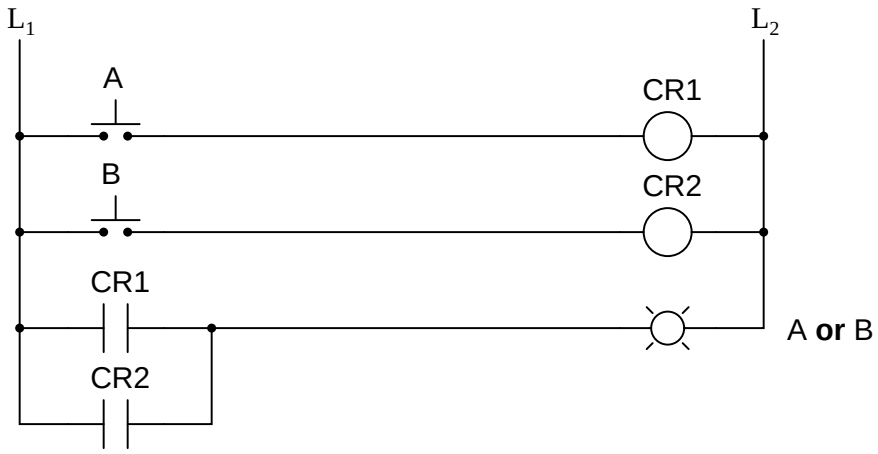


"L1" and "L2" represent the "hot" and "neutral" lines, respectively, in a 120 volt AC power system. Often, the control circuit power is obtained from a step-down transformer, which is in turn fed by a higher voltage source (usually one phase of a 480 volt AC three-phase system, in American industrial applications).

Answer 35

In ladder logic diagrams, relay coils are associated with their respective contacts by *name* rather than by proximity. In this particular circuit, the logic function represented is the AND function.

Answer 36

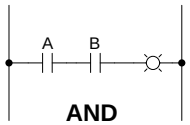


Answer 37

Truth table

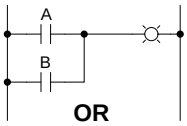
A	B	Output
0	0	0
0	1	1
1	0	0
1	1	0

Answer 38



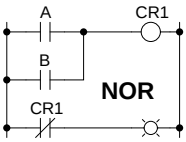
AND

A	B	Output
0	0	0
0	1	0
1	0	0
1	1	1



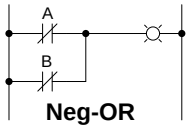
OR

A	B	Output
0	0	0
0	1	1
1	0	1
1	1	1



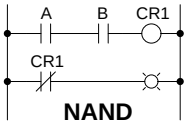
NOR

A	B	Output
0	0	1
0	1	0
1	0	0
1	1	0



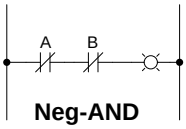
Neg-OR

A	B	Output
0	0	1
0	1	1
1	0	1
1	1	0



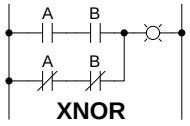
NAND

A	B	Output
0	0	1
0	1	1
1	0	1
1	1	0



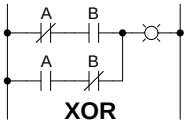
Neg-AND

A	B	Output
0	0	1
0	1	0
1	0	0
1	1	0



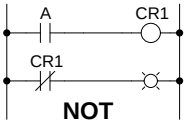
XNOR

A	B	Output
0	0	1
0	1	0
1	0	0
1	1	1



XOR

A	B	Output
0	0	0
0	1	1
1	0	1
1	1	0

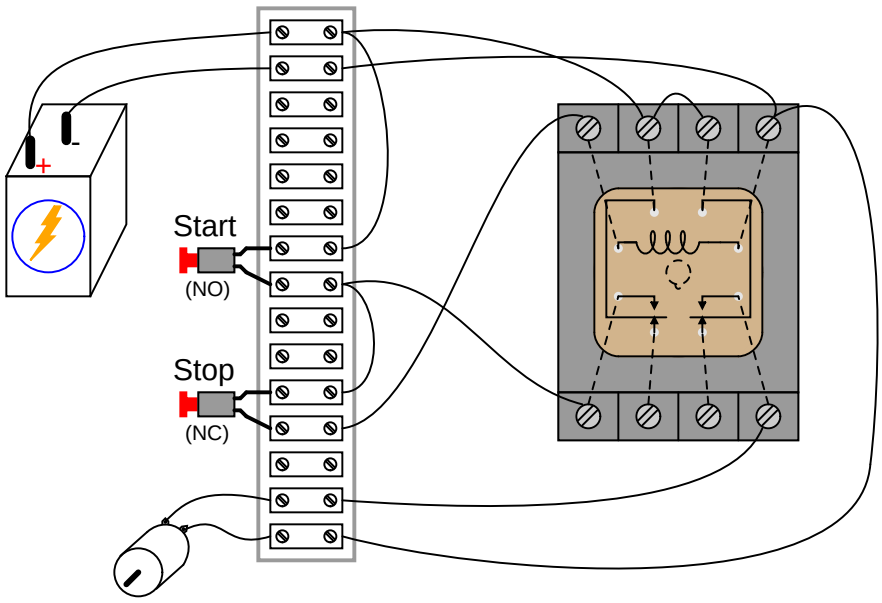


NOT

A	Output
0	1
1	0

Answer 39

The wiring sequence shown here is not the only valid solution to this problem!

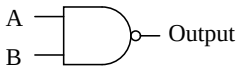


Answer 40

Never, ever connect load devices in series in a control circuit such as this!

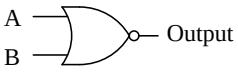
Answer 41

NAND



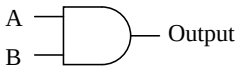
A	B	Output
0	0	1
0	1	1
1	0	1
1	1	0

NOR



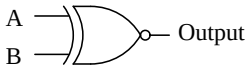
A	B	Output
0	0	1
0	1	0
1	0	0
1	1	0

AND



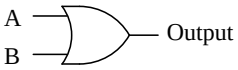
A	B	Output
0	0	0
0	1	0
1	0	0
1	1	1

XNOR



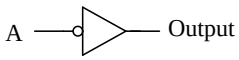
A	B	Output
0	0	1
0	1	0
1	0	0
1	1	1

OR



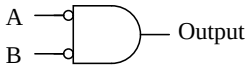
A	B	Output
0	0	0
0	1	1
1	0	1
1	1	1

NOT



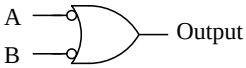
A	Output
0	1
1	0

Neg-AND



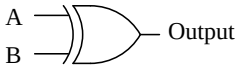
A	B	Output
0	0	1
0	1	0
1	0	0
1	1	0

Neg-OR



A	B	Output
0	0	1
0	1	1
1	0	1
1	1	0

XOR



A	B	Output
0	0	0
0	1	1
1	0	1
1	1	0

Answer 42

I_{OL} is typically much greater than I_{OH} for a TTL gate with totem-pole output circuitry. The reason for this should be obvious from inspection of the internal circuitry.

Answer 43

I'll leave the research of specific propagation time delay figures up to you! The reason propagation delay exists is because transistors cannot turn on and turn off instantaneously. In bipolar transistors, this is due to the time required to establish minority carrier flow within the base layer of the transistor (to turn it on), and to "sweep out" those minority charge carriers out of the base (to turn it off).

Follow-up questions: What difference is there between high-to-low output transitions versus low-to-high output transitions for the gate you researched? Which transition is faster?

Answer 44

A fan-out limit for TTL exists because TTL outputs have to sink current from TTL inputs in the "low" state, and their current-sinking ability is limited by the output transistor in the driving gate. If this fan-out limit is exceeded, the voltage level at the driven gate inputs may rise above the lower compliance limit.

Answer 45

Logic gates will be damaged if one tries to sink the output current sourced by another.

Answer 46

Noise margin is the difference between the acceptable voltage limits for corresponding input and output logic states.

Answer 47

I'll leave the research of specific propagation time delay figures up to you! The reason propagation delay exists is because transistors cannot turn on and turn off instantaneously. In insulated-gate field-effect transistors, this is primarily due to the time required to charge or discharge the gate-to-channel capacitance.

Follow-up questions: What difference is there between high-to-low output transitions versus low-to-high output transitions for the gate you researched? Which transition is faster?

Answer 48

A fan-out limit for CMOS exists because CMOS outputs have to source and sink *capacitive* charging and discharging current from the CMOS inputs. I'll let you determine why this limit is frequency-dependent.

Answer 49

Noise margin is the difference between the acceptable voltage limits for corresponding input and output logic states.

Answer 50

Lower operating voltages result in less power dissipation. However, noise margins become "tighter" under the same conditions, which is a disadvantage.

Answer 51

Use circuit simulation software to verify your predicted and actual truth tables.

Answer 52

Use circuit simulation software to verify your predicted and actual truth tables.

Answer 53

Use circuit simulation software to verify your predicted and actual truth tables.

Answer 54

Use circuit simulation software to verify your predicted and actual truth tables.

Answer 55

Use circuit simulation software to verify your predicted and actual truth tables.

Answer 56

Be sure you meet with your instructor if you have any questions about what is expected for your project!

Answer 57

- Diode D_1 fails open: *No effect.*
- Diode D_1 fails shorted: *Output always in high state, possible damage to circuit when input switch is in high state.*
- Diode D_2 fails open: *Gate can sink current in low output state, but cannot source current in high output state.*
- Resistor R_1 fails open: *Output always in high state.*
- Resistor R_2 fails open: *Gate can sink some current in low output state, but cannot source current in high output state. Gate may have trouble attaining a solid "low" output state as well.*
- Resistor R_4 fails open: *Limited ability to source current in high output state.*

Answer 58

- Diode D_1 fails open: *No effect.*
- Diode D_1 fails shorted: *Output always in high state, possible damage to circuit when input switch is in high state.*
- Diode D_2 fails open: *No effect.*
- Resistor R_1 fails open: *Output always in high state.*
- Resistor R_2 fails open: *Gate can sink some current in low output state, but cannot source current in high output state. Gate may have trouble attaining a solid "low" output state as well.*
- Transistor Q_2 emitter terminal fails open: *Output always in high state.*
- Transistor Q_3 emitter terminal fails open: *Gate can sink current in low output state, but cannot source current in high output state.*

Answer 59

- Diode D_1 fails open: *No effect.*
- Diode D_1 fails shorted: *Output always in low state, possible damage to circuit when input is forced low by another gate (or switch).*
- Diode D_2 fails open: *No effect.*
- Diode D_2 fails shorted: *Output always in high state, possible damage to circuit when input is forced high by another gate (or switch).*
- Transistor Q_1 fails open (drain to source): *Output cannot source current in high state, but is still able to sink current in low state.*
- Transistor Q_2 fails open (drain to source): *Output cannot sink current in low state, but is still able to source current in high state.*

Answer 60

- Transistor Q_1 failed shorted (drain to source).
- Transistor Q_4 failed open (drain to source).
- Transistor Q_5 failed open (drain to source).
- Transistor Q_{10} failed shorted (drain to source).

Answer 61

- Transistor Q_1 failed shorted (collector to emitter)
- Transistor Q_2 failed shorted (collector to emitter)
- Input line A shorted to ground
- Input line B shorted to ground
- Resistor R_{pullup} failed open

Follow-up question: though all of these faults *would* cause the output to go low, not all of them would cause the output to go low in the same way. Explain this.

Answer 62

Truth table (good circuit)

A	B	Output
0	0	0
0	1	0
1	0	1
1	1	0

Truth table (with fault)

A	B	Output
0	0	0
0	1	0
1	0	1
1	1	1

If you thought that the "faulted" truth table would be all 0's, you probably thought I said relay *contact* CR2 failed open. The fault I proposed was relay CR2 **coil** failed open.

Answer 63

- "Stop" pushbutton switch fails open: *Motor cannot start, lamp never energizes.*
- Relay contact CR1-1 fails open: *Motor starts and lamp energizes when "Start" button is pressed, but both immediately de-energize when it is released.*
- Relay contact CR1-2 fails open: *"Motor run" lamp turns on and off as expected, but the motor itself never runs.*
- Relay coil CR1 fails open: *Motor cannot start, lamp never energizes.*

Answer 64

Try checking for line voltages at the "line" (source) side of the contactor, between terminals 1 and 2, 2 and 3, and 1 and 3, with the contactor energized (motor is supposed to be running). I'll leave it to you to explain why this is a good place to check first.

Answer 65

Here are some possible faults (not an exhaustive list by any means!):

- Any fuse blown
- Contactor coil failed open
- Any transformer winding failed open
- Broken jumper between H3 and H2 on the transformer
- Corroded wire connection at terminal A1 or A2
- Motor winding failed shorted

Follow-up question: there will be a difference in operation between the L1 fuse blowing and either the L2 or L3 fuse blowing. Explain what this difference is, and why it might serve as a clue to what was wrong.

Answer 66

The chip's internal input protection diodes allowed the switch inputs to supply operating power to the MOSFET transistors.

Answer 67

Switch ON:

- Points 1 and 5: **Voltage!**
- Points 6 and 7: *No voltage*
- Points 4 and 10: *No voltage*
- Points 9 and 12: **Voltage!**
- Points 6 and 12: *No voltage*
- Points 9 and 10: *No voltage*
- Points 4 and 7: **Voltage!**

Switch OFF:

- Points 1 and 5: **Voltage!**
- Points 6 and 7: *No voltage*
- Points 4 and 10: *No voltage*
- Points 9 and 12: *No voltage*
- Points 6 and 12: **Voltage!**
- Points 9 and 10: *No voltage*
- Points 4 and 7: **Voltage!**

Follow-up question: explain *why* there will be voltage or no voltage between each of these pairs of points for the two circuit conditions (switch on and switch off).

Answer 68

Disconnect the power supply from the circuit board (only one wire need be disconnected), and then use an ohmmeter to measure continuity across the switch terminals when in the "ON" position and when in the "OFF" position. Incidentally, this is not the only way to check the switch's continuity, but it is the most direct.

Answer 69

Only two out of the four given statements are true:

1. Between two points that are electrically common to each other, there is guaranteed to be zero voltage.
4. If voltage is measured between two points, those points must not be electrically common to each other.

For those having difficultly understanding this, test the following statements for truth. Each of these statements follows the same logical pattern of electrical statements given at the beginning of this question:

1. All rabbits are mammals.
2. All mammals are rabbits.
3. All non-rabbits are non-mammals.
4. All non-mammals are non-rabbits.

Answer 70

- Slight sensation at point(s) of contact: **1.85 volts**
- Threshold of bodily perception: **4.3 volts**
- Pain, with voluntary muscle control maintained: **36.9 volts**
- Pain, with loss of voluntary muscle control: **64.6 volts**
- Severe pain and difficulty breathing: **92.3 volts**
- Possible heart fibrillation after three seconds: **615 volts**

Answer 71

- Point "A" *dangerous to touch*
- Point "B" *dangerous to touch*
- Point "C" *dangerous to touch when motor is turned on*
- Point "D" *safe to touch*
- Point "E" *safe to touch*

Answer 72

These are all interesting points to consider as a group. I'll let you figure out possible answers to these questions together in class.

Answer 73

A tag informs anyone wishing to turn the disconnect device "on" as to *when* it was turned off, and *who* placed the lock(s) on it. Many lockout tags have space on for a written description so that the reason for the lockout may be explained.

Answer 74

You should check the equipment site to be sure no one is still working on it, unaware of the impending startup.

Answer 75

The circles with dots show the magnetic flux vectors coming at you from out of the paper. The circles with crosses show the magnetic flux vectors going away from you into the paper. Think of these as images of arrows with points (dots) and fletchings (crosses).

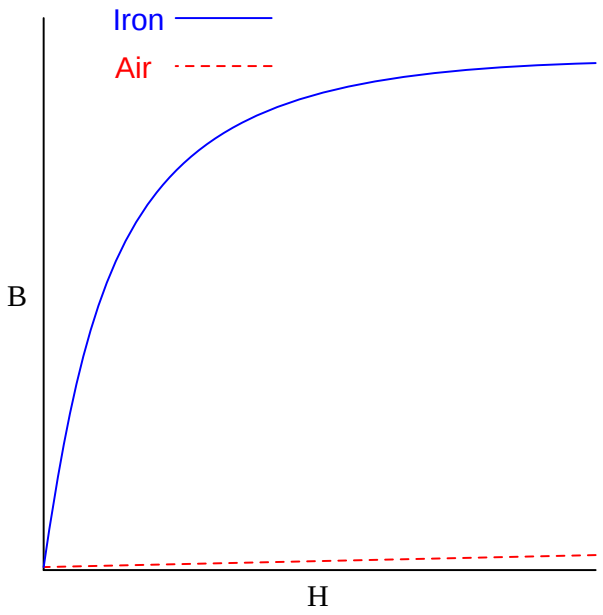
Answer 76

- Meter A = 2.5 amps
- Meter B = 2.5 amps
- Meter C = 0 amps

Answer 77

$$\Phi = \frac{NI}{\Re}$$

Answer 78



Follow-up question: note that the slope of both plots are approximately equal toward the far right end of the graph. Explain this effect in terms of magnetic *saturation*.

Answer 79

3.6 volts

Answer 80

The disk's own magnetic field will develop in such a way that it "fights" to keep a constant distance from the magnet:

Figure 1

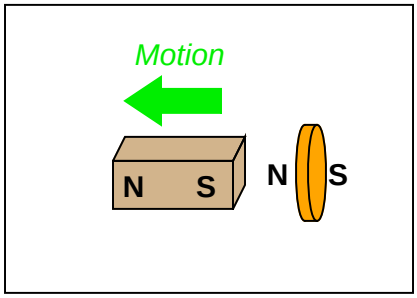


Figure 2

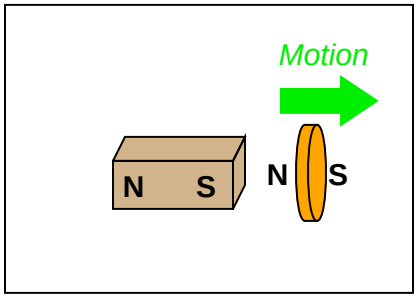


Figure 3

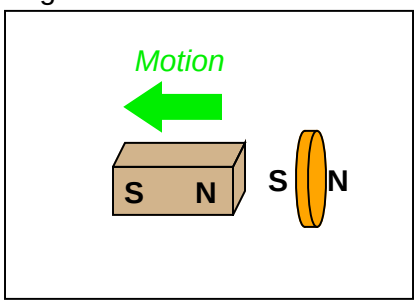
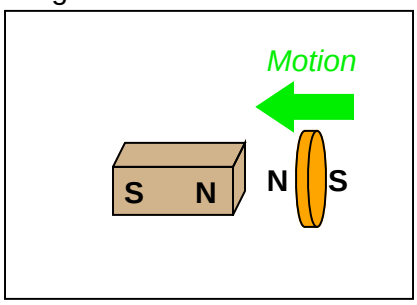


Figure 4



Follow-up question: trace the direction of rotation for the induced electric current in the disk necessary to produce both the repulsive and the attractive force.

Answer 81

Note: in case it isn't clear from the illustrations, Figures 1 through 4 show the magnet moving in relation to a stationary coil. Figures 5 and 6 show a coil moving in relation to a stationary magnet.

Figure 1

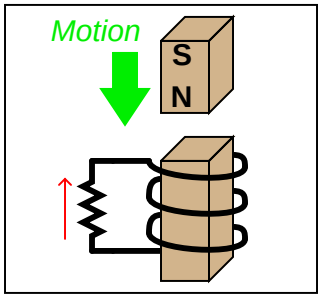


Figure 2

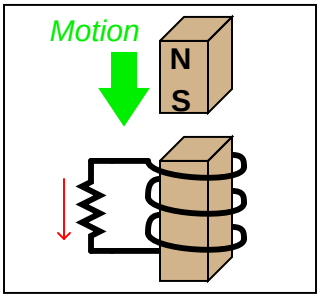


Figure 3

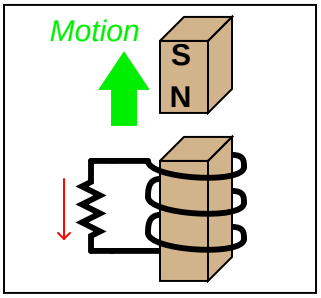


Figure 4

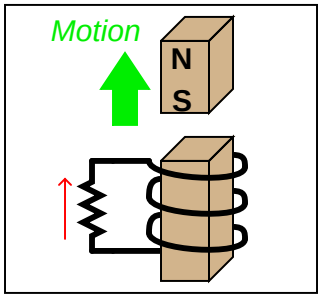


Figure 5

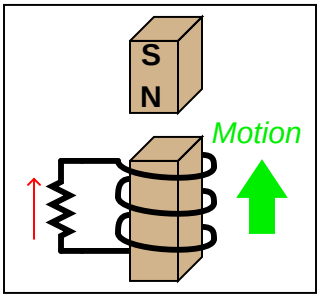
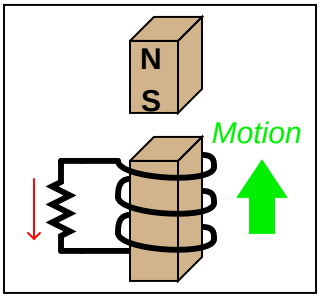
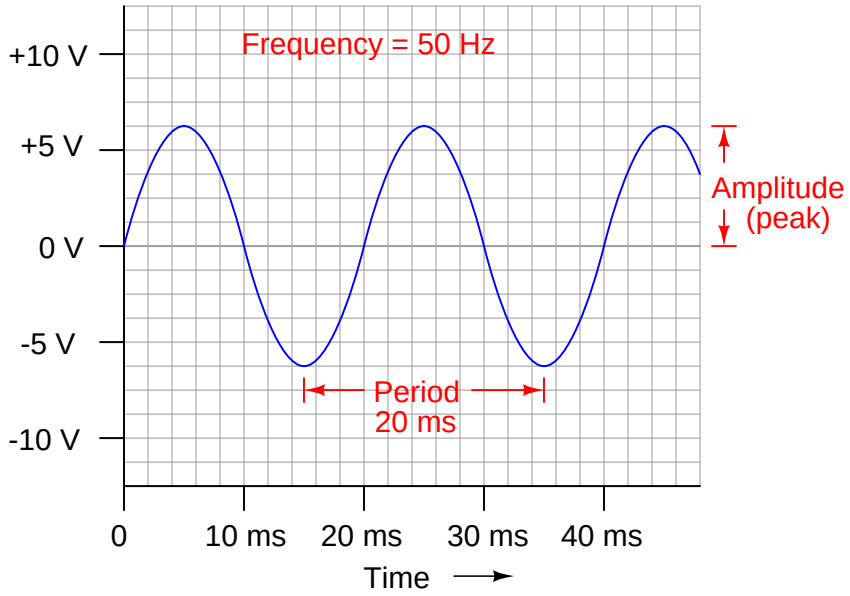


Figure 6



Note: all current directions shown using conventional flow notation (following the right-hand rule)

Answer 82



Answer 83

$\lambda \approx 316$ meters

I'll let you find the equation on your own!

Answer 84

The RMS amplitude of this waveform is approximately 0.32 volts.

Answer 85

The RMS amplitude of this waveform is 0.5 volt.

Answer 86

$\Theta \approx 34.5^o$

Answer 87

I'll let you do your homework on this question!

Answer 88

Ease of configuration and flexibility!

Answer 89

A "loop" is necessary for the MCU to repeat the on/pause/off sequence. What is needed now is another time delay within the loop:

Pseudocode listing

```
Declare Pin0 as an output
LOOP
  Set Pin0 HIGH
  Pause for 1 second
  Set Pin0 LOW
  Pause for 1 second (new line of code)
ENDLOOP
```

Answer 90

The conditional "WHILE" loop needs to be placed inside an unconditional loop:

Pseudocode listing

```
Declare Pin0 as an output
Declare Pin1 as an input
LOOP
  WHILE Pin1 is HIGH
    Set Pin0 HIGH
    Pause for 0.5 seconds
    Set Pin0 LOW
    Pause for 0.5 seconds
  ENDWHILE
ENDLOOP
```

Follow-up question: what purpose does the resistor $R_{pulldown}$ serve in the pushbutton circuit?

Answer 91

This microcontroller implements the logical OR function.

Answer 92

This microcontroller implements the logical AND function.

Answer 93

This microcontroller implements the logical NAND function.

Answer 94

This microcontroller implements the logical NOR function.

Answer 95

This microcontroller implements the logical Exclusive-OR function.

Answer 96

This microcontroller implements the logical Exclusive-NOR function.

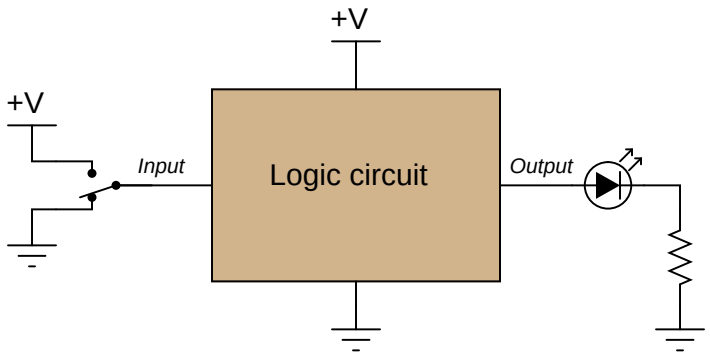
Answer 97

- Resistance of a rheostat: *continuous*
- Resistance of a switch: *discrete*
- Time represented by an analog clock: *continuous*
- Time represented by a digital clock: *discrete*
- Quantity of money in a billfold (bills and coins): *discrete*
- Number of pebbles held in a hand: *discrete*
- A person's weight, in pounds or kilograms: *continuous*
- Voltage output by a comparator: *discrete*
- Voltage output by an operational amplifier: *continuous* (if negative feedback is applied)
- Electrical conductivity of a thyristor: *discrete*

Answer 98

Slide rules are analog, while abaci (abacuses?) are digital.

Answer 99



Answer 100

This is an OR gate circuit.

Answer 101

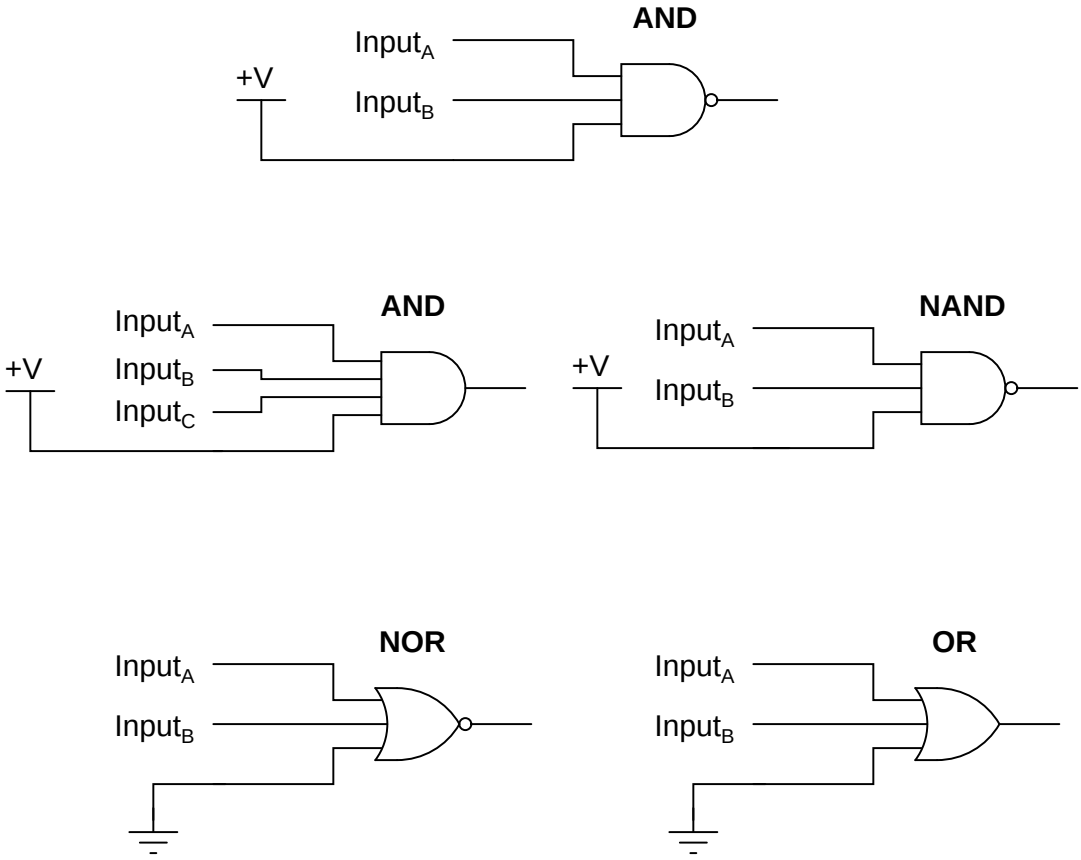
- Any high input guarantees a low output: **NOR** gate.
- Any low input guarantees a high output: **NAND** gate.
- Any low input guarantees a low output: **AND** gate.

Answer 102

A	B	C	Output
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	1

Follow-up question: how do you suppose the truth tables would look like for three-input OR, NOR, and NAND gates? Explain how one may transition from the regular two-input gates to gate circuits with more than two inputs. What remains the same despite additional input lines?

Answer 103



Answer 104

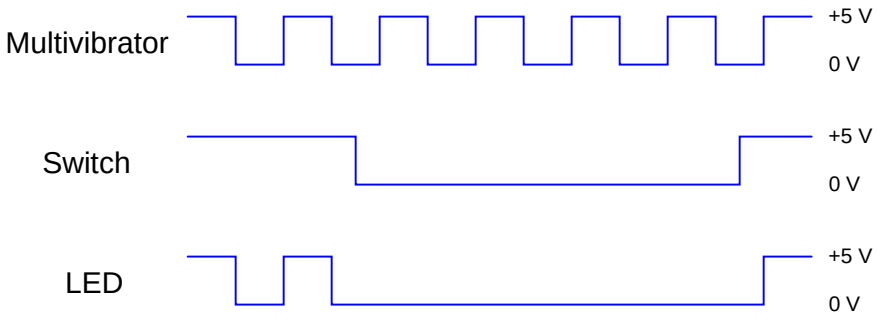
V_{CC} = Power supplied to collector side of bipolar transistors.
V_{EE} = Power supplied to emitter side of bipolar transistors.

Follow-up question: Since TTL circuits use NPN transistors exclusively, what polarities must each of these labels represent?

Answer 105

I'll let you do your own research on this question. DO NOT obtain your answer from a textbook, but consult a manufacturer's datasheet instead!

Answer 106



Answer 107

The "S" figure, which resembles a magnetic B-H hysteresis curve, marks this gate as a *Schmitt trigger*. I'll let you do the research to determine what this means in regard to gate function.

Answer 108

The labels V_{DD} and V_{SS} are supposed to mean "power supply to *drain* and *source* sides of MOSFETs, respectively. This nomenclature is actually a holdover from obsolete NMOS gate designs, which used N-channel MOSFETS exclusively. Even though it doesn't make much sense in CMOS circuits (you'll see why if you examine the internal schematic diagram for a CMOS gate), it is the standard way of denoting power supply terminals for CMOS circuits.

Follow-up question: what polarities do these respective labels represent?

Answer 109

In this particular case, the way the load (LED) is connected to the output of the gate, the gate will only *sink* current. However, the gate is capable of sourcing current to a load, if only the load were connected differently.

Follow-up question: re-draw the circuit to show the gate *sourcing* current to an LED load.

Answer 110

If you thought the answer to this question was, "because MOSFET transistors are immune to damage from high-voltage transients," you were wrong. If anything, MOSFETs are even more susceptible to damage from high-voltage transients than BJTs, given their thinly insulated gates.

The correct answer has to do with the *bilateral* (non polarity-sensitive) nature of MOSFETs when conducting. Trace the direction of current through the relay coil while energized, and at the point in time when the gate output switches to a "low" state, and you will understand why no commutating diode is necessary in this circuit.

Answer 111

If an input or output of a CMOS gate circuit is driven above V_{DD}, even momentarily, the circuit may "latch" like an SCR, causing V_{DD} to become shorted to V_{SS} internally. This is made possible by the way CMOS transistors are manufactured on the integrated circuit's substrate.

Challenge question: referencing a cross-sectional illustration of a CMOS gate integrated circuit, show the "SCR" formed by the transistors, and explain how it may be "fired" by excessive input voltage to the gate.

Answer 112

The conductive foam makes the pins electrically common to one another, so no significant *difference* of voltage may appear between any two pins of the component.

Answer 113

One of the most significant differences is that in ladder diagrams, relay coils and relay contacts (the normally-open contact in this diagram shown as a capacitor-like symbol) need not be drawn near each other.

Follow-up question: what do the two labels "L1" and "L2" represent?

Answer 114

The "Run" switch is a normally-open pushbutton. Relay coil "M1" is energized by this switch, and actuates three normally-open contacts (also labeled "M1") to send three-phase power to the motor. Note that the details of the power supply are not shown in these diagrams. This is a common omission, done for the sake of simplicity.

Answer 115

In this circuit, the motor will start once the "Run" switch is actuated. When the "Run" switch is released, the motor continues to run.

Follow-up question: this circuit has no "stop" switch! What would have to be modified in the ladder logic circuit to provide "stop" control?

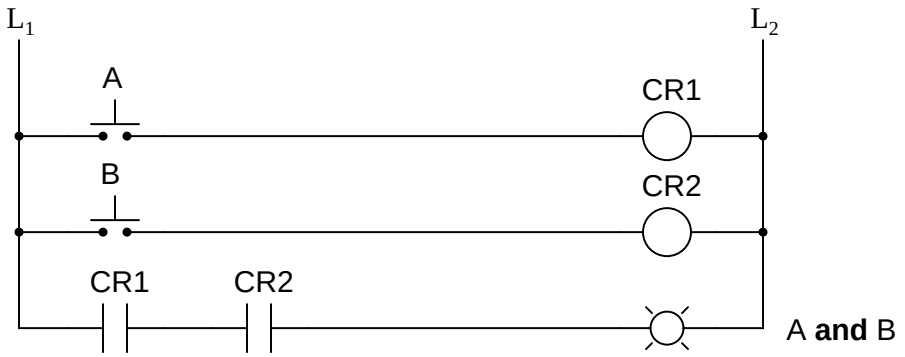
Answer 116

"Form C" is just another way of saying "SPDT" with regard to switch or relay contacts.

Answer 117

In a properly designed system, with L2 grounded at the power source, this fault will result in a blown fuse when the pressure switch closes. In a circuit with L1 and L2 reversed, this same ground fault would energize the relief solenoid, with or without the pressure switch's "permission."

Answer 118



Answer 119

Lamp 1

A	B	Output
0	0	1
0	1	0
1	0	0
1	1	0

Lamp 2

A	B	Output
0	0	1
0	1	0
1	0	0
1	1	0

Each of the lamps exhibits the behavior of a "NOR" gate.

Notes

Notes 1

The purpose of this question is to get students thinking in terms of "digital" quantities, which by their very nature are non-continuous. Since most electronics curricula focus on continuous quantities before discrete, it is good to have students reflect on the inherent simplicity of discrete circuitry and components after having studied continuous (analog) circuitry.

Notes 2

This is a very simple concept, but worthwhile to cover in its own question just to be sure no students misunderstand when the concept is later applied.

Notes 3

This question applies the concepts of "high" and "low" voltage signals to a simple transistor circuit, reviewing transistor operation in the process.

Notes 4

If students do not understand the purpose of these resistors after reading the question and researching their texts, they should when they see the follow-up question. Discuss this question with your students, for the concept of pulldown and pullup resistors is one that confuses some students.

Notes 5

This is one concept I have found many students have difficulty grasping, essentially because it involves the determination of a voltage drop between two points (the "arrow" wire and ground). It is a spatial-relations problem, similar to Kirchhoff's Voltage Law problems where students need to figure out how much voltage is between two specified points given voltage drops across several other pairs of points. Spend time with your students discussing these circuits, because several of your students will probably not understand this concept the first, second, or even third time through.

I strongly recommend students take the approach of a "thought experiment" in determining the efficacy of each circuit shown here: analyze the output voltage (logic state) for each of the switch's two positions. This simple approach usually helps clarify what each circuit does and why the "improper" circuits do not work.

Notes 6

It is important for students to understand that there is a certain range of voltage between a guaranteed "high" state and a guaranteed "low" state that is indeterminate, and that this logic probe circuit is designed to indicate this range of voltage by turning neither LED on.

If time permits, discuss some of the benefits and drawbacks to using a voltmeter as a logic probe (especially a *digital* voltmeter where the display update time may be relatively long).

Notes 7

Your students should have no great difficulty identifying this particular logic gate if they have a good digital electronics reference book at their disposal.

Notes 8

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Notes 9

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Notes 10

Diode-resistor gate circuits such as this are rarely used in real digital circuitry because they have no capacity to *amplify* weak input signals. They also have no capacity for signal inversion, rendering them incapable of representing a great many logic function types. Gates made from transistors are much preferred over diode-resistor technology.

Notes 11

In order to familiarize students with the standard logic gate types, I like to given them practice with identification and truth tables each day. Students need to be able to recognize these logic gate types at a glance, or else they will have difficulty analyzing circuits that use them.

Notes 12

Have your students explain the operation of this TTL circuit, describing how the inverse logic state is generated at the output terminal, from a given input state.

Notes 13

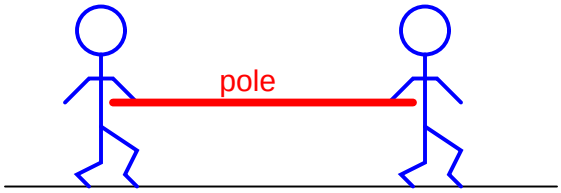
TTL circuits are actually quite easy to analyze compared to analog amplifier circuits! Discuss with your students the use of a dual-emitter transistor as a "steering" diode network: this is a trick used by IC manufacturers, to obtain three diodes for the "price" of one transistor.

Notes 14

The very important concept of sourcing versus sinking is best understood from the perspective of *conventional* current flow notation. The terms seem backward when electron flow notation is used to track current through the output transistor.

One point of confusion I've experienced among students is that current may go either direction (in or out) of a gate with totem-pole output transistors (able to sink or source current). Some students seem to have a conceptual difficulty with current going *in* to the *output* terminal of a gate circuit, because they mistakenly associate the "out" in *out*put as being a reference to direction of current, rather than direction of information or data.

An analogy I've used to help students overcome this problem is that of two people carrying a long pole:



Suppose these people are in a dark, noisy room, and they use the pole as a means of simple communication between them. For example, one person could tug on the pole to get the other person's attention. Perhaps they could even develop a simple code system for communicating thoughts (1 tug = hello ; 2 tugs = good-bye ; 3 tugs = I think this is a silly way to communicate ; 4 tugs = let's leave this room ; etc.). If one of the persons *pushes* on the pole rather than *pulls* on the pole to get the other person's attention, does the direction of the pole's motion change the direction of the communication between the two persons? Of course not. Well, then, does the direction of current through the output terminal of a gate change the direction that *information* flows between two interconnected gates? Whether a gate sources current or sinks current to a load has no bearing on the "output" designation of that gate terminal. Either way, the gate is still "telling the load what to do" by exercising control over the load current.

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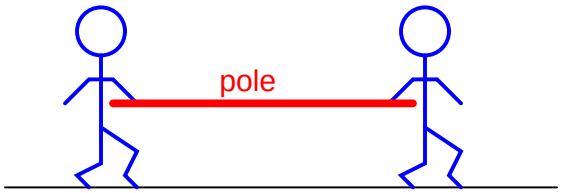

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Ask your students to explain what the term "open-collector" means with reference to a TTL logic gate. How does this type of gate compare with normal ("totem pole" output) TTL gates?

Notes 16

For review, ask your students what the symbols V_{CC} and V_{EE} mean with reference to TTL circuits.

Proper TTL "etiquette" is vitally important for students to understand, if they are to successfully build digital circuits (especially when interfacing TTL with other types of logic!).

Notes 17

The most obvious lesson of this question is to introduce (or review as the case may be) the purpose and operation of a logic probe. However, this question is also a veiled introduction (or review) of TTL logic levels.

Notes 18

Discuss the problem of "floating" or "high-Z" states with your students. It is always a good idea to eliminate ambiguous logic states such as this in the circuits you build.

Notes 19

The utility of conventional flow notation (as opposed to electron flow) becomes especially apparent in this answer, as the upper circuit is the one *sourcing* current and the lower circuit is the one *sinking* current.

As with operational amplifiers, I find it necessary to point out to some students that the inputs of a logic gate circuit do not sink or source load current. This fact underscores the need to supply DC power to the logic gate for proper operation.

Notes 20

Ask your students why we might want to use a Darlington pair instead of a single transistor for the final output "driver" circuit. Also, ask them why we need to have a resistor connected between the gate output and the transistor base. Why not just directly connect the gate's output to the base of the transistor?

You might want to challenge your students with this question: "Suppose the person who built this circuit used open-collector gates throughout. As a whole, it would not function, neither for lighting the LED nor for ringing the bell. However, only one of the gates would need to have the standard 'totem-pole' output in order for the circuit to function properly. Which gate is it?"

Notes 21

In order to familiarize students with the standard logic gate types, I like to given them practice with identification and truth tables each day. Students need to be able to recognize these logic gate types at a glance, or else they will have difficulty analyzing circuits that use them.

Notes 22

Have your students explain the operation of this very simple MOSFET circuit, describing how the inverse logic state is generated at the output terminal, from a given input state. Discuss with your students the simplicity of the CMOS inverter, especially contrasted against a TTL inverter circuit.

Notes 23

It is important that students realize these "protection" diodes do not allow circuit designers and builders to disregard good design practices with impunity. Ask your students, in each case, how each protection diode accomplishes its task of protecting the MOSFETs from damage. Does this mean the gate circuit will be able to withstand abnormal conditions indefinitely? Why or why not?

Notes 24

Discuss the problem of "floating" or "high-Z" states with your students, especially in the context of CMOS. What is it about the nature of a CMOS circuit that makes floating inputs especially troublesome? Ask your students to contrast this against floating TTL inputs.

Notes 25

CMOS logic gate circuits are the easiest of all the gates to analyze internally! Discuss with your students why the second-from-the-top MOSFET uses an independent substrate connection (as opposed to making it common with the source, as usual).

Notes 26

This question gets students in the habit of consulting datasheets to obtain information on logic gate circuits. Datasheets are a wealth of technical information, and students absolutely have to become adept at referencing them to obtain the information they need to build and troubleshoot logic circuits.

Notes 27

The most obvious lesson of this question is to introduce (or review as the case may be) the purpose and operation of a logic probe. However, this question is also a veiled introduction (or review) of CMOS logic levels.

Notes 28

I strongly suggest you take the time to implement an improved-security design with your students. A practical project such as this sparks a lot of interest, and thus provides an excellent learning opportunity.

Not only does this question afford the opportunity to analyze logic gates, but it also provides a context in which to review optocouplers and TRIACs. Ask your students what the labels "L1" and "L2" mean, with reference to AC power circuitry, as well.

Notes 29

Texas Instruments publishes an excellent application report (SCHA004 – October 2002) comparing buffered versus unbuffered CMOS logic gates. I highly recommend it for your reference.

Notes 30

High-speed CMOS was a very important developmental milestone in digital logic gate technology, and it is essential for modern (2005) students of electronics to be aware of since it is so widely used. In many ways it blends the best of the old TTL and CMOS worlds, with few disadvantages.

Notes 31

This question provides a good opportunity to review electromechanical relays: how they work, what they are used for, etc.

Notes 32

Ask your students to identify what arrangement the relay contacts are connected it: series or parallel? Does this contact arrangement make sense with regard to the established function of the gate?

Notes 33

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Notes 34

If students don't raise this point on their own, direct their attention to the relay coil and contact symbols. What looks strange here? What sort of electrical component are students familiar associating with the "CR1" contact symbol? Does it make sense to use this symbol to symbolize a normally-open switch (relay) contact? If we wished to show a normally-closed relay contact instead, how would we modify the diagram?

Notes 35

Many students find it confusing that relay contacts and coils need not be drawn next to one another in a ladder logic diagram, because it is so different from the schematic diagrams they are accustomed to. The non-necessity of proximity in a ladder logic diagram does have its advantages, though! It is simply a matter of getting used to a new way of drawing things.

Notes 36

Discuss with students the fact that relay coils and contacts need not be located near each other in ladder diagrams. While this may be confusing at times, it is a very flexible feature of ladder logic notation, because it gives the author the freedom to locate relay contacts where it makes the most visual sense in the "output" rung of the diagram, without having to coordinate locations of coil and contact as is generally necessary in traditional schematic diagrams. Instead, relay contacts are associated with their respective coils *by label*, not by proximity on the diagram.

Notes 37

Many students find the "line-through-the-contact" a very intuitive way to represent normally-closed relay contacts. Be sure to emphasize that the diagonal line, as well as the name *normally*-closed, does not refer to any given state of the contact, but rather to the contact's *resting* state when the relay coil is de-energized. I have seen teachers put a diagonal line through a relay contact symbol on a ladder logic diagram to indicate the state of the contact being closed by energization of the coil, during the process of explaining how a circuit functioned. This is wrong, as it confuses the concept of contacts being normally-closed with the concept of contacts simply being (energized) closed.

Notes 38

In order to familiarize students with standard switch contact configurations, I like to given them practice with identification and truth tables each day. Students need to be able to recognize these ladder logic sub-circuits at a glance, or else they will have difficulty analyzing more complex relay circuits that use them.

Notes 39

This circuit provides students with an opportunity to analyze a simple *latch*: a system that "remembers" prior switch actuations by holding a "state" (either set or reset; latched or unlatched). A simple motor start/stop circuit such as this is about as simple as latch circuits get.

Students should be able to immediately comprehend the benefit of using nice, neat, structured ladder diagrams when they see the tangled mess of wires in a real motor control circuit. And this is not even a complex motor control circuit! It takes very little imagination to think of something even uglier than this, and what a task it would be to troubleshoot such a circuit without the benefit of a ladder diagram for guidance.

Notes 40

Discuss with your students why load devices are never to be connected in series. What would be the effect of doing so? Have them answer this question in terms of normal operation, and also in terms of operation given a failure condition in one of the series-connected load devices.

Notes 41

In order to familiarize students with the standard logic gate types, I like to given them practice with identification and truth tables each day. Students need to be able to recognize these logic gate types at a glance, or else they will have difficulty analyzing circuits that use them.

Notes 42

It should be noted that totem-pole TTL gates can actually source far more current than what is advertised without sustaining damage. The severe limitation on sourcing current is more a function of staying within the permitted output voltage margins for TTL than it is a function of chip heating. Thus, you may generally use a totem-pole TTL gate to source 20 mA to an LED without harm, though the "high" state output voltage (when the LED is lit) will be significantly below the acceptable threshold for a TTL gate *input*.

Notes 43

I purposely omitted answers for this question, not only because I want students to do the research on their own, but also because it makes it more interesting when students consult different datasheets and derive different answers (for different logic "families")!

Notes 44

For the relatively simple digital circuits that beginning students build, fan-out is rarely a problem. More likely is that students will try to drive a load that is too "heavy," causing the same voltage level problem.

Notes 45

The given answer cuts to the heart of the matter, but I want students to elaborate on the details. Specifically, why each of the three acceptable paralleled circuits avoids risk of damage. Make sure you spend adequate time discussing "tri-state" outputs as well. Ask your students to explain what the three output states of a "tri-state" gate are.

Notes 46

This question, to be answered properly, involves more than just a definition of "noise margin." Students must first discover that there is a difference between voltage compliance levels for gate inputs versus outputs, then recognize that the difference constitutes a "margin" that imposed AC voltage ("noise") must not exceed. They must then present their answer in terms of manufacturer specifications, obtained in datasheets. In summary, there is a lot of research that must occur to answer this question, but the results will be worth it!

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Notes 50

Discuss this trend with your students, citing examples from industry literature if possible. Be sure to ask your students *why* lower operating voltages reduces power dissipation (with reference to Joule's Law, please!), and also why this reduces noise margins.

Notes 51

The choice of diodes is not critical in a circuit where the inputs come from manually actuated switches. Neither is the choice of resistor sizes (10 kΩ) works just fine, especially when the only thing loading the output is the student's logic probe or voltmeter.

Notes 52

It needs to be understood that this is an AND gate only if you consider the "0" and "1" states as defined by voltage levels with respect to ground, and not by switch actuation. Many students assume an actuated (pushed) switch is a "1" input and a de-actuated (unpushed) switch is a "0" input. Not necessarily so! In this circuit, the switches are connecting inputs to *ground*. This means a closed (actuated) switch provides a low (0) input state, while an open (unactuated) switch provides a high (1) input state.

Notes 53

The purpose of this exercise is for students to research what type of IC this is (from the given part number for U_1), its pinout, and then predict and prove its operation using truth tables to document the results. You, as the instructor, may select any 14-pin CMOS or TTL logic IC that you wish. Students are to draw the logic gate symbol within the rectangle of U_1, then connect that symbol to the input switches and output LED.

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Notes 54

The transition from ladder logic diagram to actual relay wiring is a confusing one for many students. This is what I consider to be the most significant learning objective of this exercise: figuring out how to build the circuit, not necessarily understanding the logical function of it.

Notes 55

Something omitted from too many basic digital electronics texts is a thorough discussion on interfacing IC logic gates with high-power devices, usually using relays. This is a very important subject, however, because many devices we wish to control with digital logic circuits are too power-hungry to directly drive with the logic gate outputs! Here, students get the opportunity to experiment with how to make a logic gate (CMOS, preferably) drive an electric motor.

One component value you may wish to have your students size themselves is resistor R_3, being the base current limiting resistor for transistor Q_1. It must be sized such that the transistor is saturated with the gate output in the HIGH state, yet not allowing so much base current that the transistor becomes damaged. Figuring out an appropriate size for this resistor is a very practical exercise, forcing students to review transistor theory (calculations with β) as well as consider characteristics of the load.

It may be advisable (especially if the logic gate is TTL and requires a precise 5.0 volt power supply) to have a separate source of power for the electric motor.

Notes 56

The purpose of this assessment rubric is to act as a sort of "contract" between you (the instructor) and your student. This way, the expectations are all clearly known in advance, which goes a long way toward disarming problems later when it is time to grade.

Notes 57

The purpose of this question is to approach the domain of circuit troubleshooting from a perspective of knowing what the fault is, rather than only knowing what the symptoms are. Although this is not necessarily a realistic perspective, it helps students build the foundational knowledge necessary to diagnose a faulted circuit from empirical data. Questions such as this should be followed (eventually) by other questions asking students to identify likely faults based on measurements.

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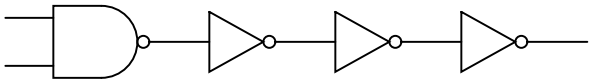
Notes 60

One way for students to approach this problem is to re-draw the schematic in gate symbol form, a NAND gate followed by three inverters:



Discuss with them why this approach may be helpful in determining possible component faults in the integrated circuit.

Notes 61

Discuss your students' answers with everyone in class, and their reasoning behind them.

Notes 62

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Notes 64

Discuss with your students the various options they have in diagnostic steps, and what they think of the step proposed in the answer. Troubleshooting scenarios such as this as excellent for stimulating active class discussions, so take advantage of it!

Notes 65

Identifying multiple faults should be quite easy in this circuit. The real value of this question is the opportunity for explanation and discussion that it generates for your students as they share their answers with each other.

Notes 66

As an instructor of electronics, I've seen students make this mistake countless times. What is particularly troublesome about this error is the seemingly intermittent behavior of the chip. Without power supplied to the chip, most students assume there would be no function at all. So when they see the chip functioning adequately in some of its circuit's states, they are inclined to assume power is not an issue!

Notes 67

This question is not really a troubleshooting question per se, but the principles involved in successfully determining the presence or absence of voltage are critically important to being able to troubleshoot simple circuits using a voltmeter.

I have found that the concept of *electrically common points* is most helpful when students first learn to relate voltage drop with continuity (breaks or non-breaks) in a circuit. You might want them to identify which points in this circuit are electrically common to one another (in either or both switch positions).

Notes 68

Challenge your students to think of other methods which could be used to check the switch's continuity. There is often more than one way to perform a certain check of component function, if you are knowledgeable in electrical theory and creative in your use of test equipment!

Notes 69

What we have here is an exercise in Aristotelian logic. In either scenario (points in a circuit, or animals), statement 2 is the *converse* of statement 1, while statement 3 is the *inverse* and statement 4 is the *contrapositive*. Only the contrapositive of a statement is guaranteed to share the same truth value as the original statement.

This is no esoteric exercise. Rather, it is a hard-learned fact: many students mistakenly think that because there is guaranteed to be no voltage between electrically common points in a circuit, then the absence of voltage between two points must mean those two points are electrically common to each other! This is not necessarily true, because situations exist where two points may not be electrically common, yet still have no voltage between them.

The contrapositive of this rule, however, is a valuable troubleshooting tool: if there is substantial voltage measured between two points in a circuit, then we know without a doubt that those two points are *not* electrically common to each other!

Notes 70

Not only does this question introduce students to the various levels of shock current necessary to induce deleterious effects in the (healthy) human body, but it also serves as a good exercise for Ohm's Law, and for introducing (or reviewing) the concept of series resistances.

For the morbidly curious, Charles Dalziel's experimentation conducted at the University of California (Berkeley) began with a state grant to investigate the bodily effects of sub-lethal electric current. His testing method was as follows: healthy male and female volunteer subjects were asked to hold a copper wire in one hand and place their other hand on a round, brass plate. A voltage was then applied between the wire and the plate, causing electrons to flow through the subject's arms and chest. The current was stopped, then resumed at a higher level. The goal here was to see how much current the subject could tolerate and still keep their hand pressed against the brass plate. When this threshold was reached, laboratory assistants forcefully held the subject's hand in contact with the plate and the current was again increased. The subject was asked to release the wire they were holding, to see at what current level involuntary muscle contraction (tetanus) prevented them from doing so. For each subject the experiment was conducted using DC and also AC at various frequencies. Over two dozen human volunteers were tested, and later studies on heart fibrillation were conducted using animal subjects.

Given that Dalziel tested subjects for the effects of a hand-to-hand shock current path, his data does not precisely match the scenario I show in the schematic diagram (hand-to-foot). Therefore, the calculated voltages for various hand-to-foot shock conditions are *approximate only*.

Notes 71

One suggestion for approaching this question is to ask your students to identify which of the power source conductors is "hot" and which one is "neutral," then identify which points in the circuit are electrically common to either one or the other source conductors.

Notes 72

The italicized text was taken directly from Puget Sound Energy's April 2005 "Energywise" mail flyer. The points brought up were, I thought, very appropriate for discussion of electrical safety and theory. Personally, I question the suggestion of shuffling on both feet. I would suspect that running full-speed, where only one foot touches the ground at a time, and where you would leave the dangerous area faster, would be the safest option. I would be very interested to see if there is any scientific test data available on this subject!

Notes 73

Discuss with your students the need for good communication between all people performing maintenance work on large and (potentially) dangerous systems. Tags are an integral part of this communication.

Notes 74

Real-life story here: I was once asked to place an electric motor back in service after it had been locked out for a few days, for routine maintenance. I removed my lock and tag, and was just about to turn the breaker back on, when better judgment prevailed and I decided to first check the job site. Lo and behold, there, still working on the motor coupling, were two contract employees completely oblivious to the situation. They had not been told there was a circuit breaker to secure power to that electric motor, nor were they aware that they needed to lock it out in addition to everyone else on the project! Had I turned that circuit breaker back on, the motor could have started up and severely injured at least one of them!

Lesson to be learned: if you are performing work on a piece of equipment, *you* need to have *your* lock and *your* tag securing energy to that equipment. Never, ever trust someone else to lock-out and tag-out a circuit breaker for you!

Notes 75

As a follow-up to this question, you might wish to draw current-carrying wires at different angles, and with current moving in different directions, as practice problems for your students to draw the corresponding arrow points and tails.

Notes 76

Clamp-on meters are very useful pieces of test equipment, but they must be used properly. I have seen many people make the mistake of clamping one of these ammeters around multiple wires when trying to measure the amount of current through only one. If you have any clamp-on meters in your classroom, have your students set up a simple circuit like this and prove the validity of the concept.

Notes 77

This is an exercise in algebraic substitution. Students are not likely to find this equation anywhere, so they'll have to create it from a combination of two other equations.

Notes 78

The purpose of this question is twofold: to get students to see that a ferromagnetic material such as iron is *much* more permeable (less "reluctant") than air, but that the great gains in B realized by iron tend to disappear as soon as saturation sets in. Once the iron is saturated, the gains in B for equal advances in H are the same as for air. That is, the $\frac{dB}{dH}$ for iron is equal to the $\frac{dB}{dH}$ for air once the iron is saturated.

Notes 79

This is simply a quantitative application of Faraday's Law. There is no significance to the fact that the magnetic flux is increasing rather than decreasing. The only effect this would have on the induced voltage is its polarity.

Notes 80

This phenomenon is difficult to demonstrate without a very powerful magnet. However, if you have such apparatus available in your lab area, it would make a great piece for demonstration!

One practical way I've demonstrated Lenz's Law is to obtain a rare-earth magnet (*very* powerful!), set it pole-up on a table, then drop an aluminum coin (such as a Japanese Yen) so it lands on top of the magnet. If the magnet is strong enough and the coin is light enough, the coin will gently come to rest on the magnet rather than hit hard and bounce off.

A more dramatic illustration of Lenz's Law is to take the same coin and spin it (on edge) on a table surface. Then, bring the magnet close to the edge of the spinning coin, and watch the coin promptly come to a halt, without contact between the coin and magnet.

Another illustration is to set the aluminum coin on a smooth table surface, then quickly move the magnet over the coin, parallel to the table surface. If the magnet is close enough, the coin will be "dragged" a short distance as the magnet passes over.

In all these demonstrations, it is significant to show to your students that the coin itself is not magnetic. It will not stick to the magnet as an iron or steel coin would, thus any force generated between the coin and magnet is strictly due to *induced currents* and not ferromagnetism.

Notes 81

An easy way I find to remember Lenz's Law is to interpret is as *opposition to change*. The coil will try to become a magnet that fights the motion. A good way to get students thinking along these lines is to ask them, "What magnetic polarity would the coil have to assume (in each case) to resist the magnet's relative motion?" In other words, if the magnet moves closer to the coil, the coil will "magnetize" so as to push against the magnet. If the magnet moves away from the coil, the coil will "magnetize" so as to attract the magnet.

Notes 82

As always, it is more important to be able to apply a term to a real-life example than it is to memorize a definition for that term. In my experience, many students prefer to memorize definitions for terms rather than to go through the trouble of understanding how those terms apply to real life. Make sure students realize just how and why these AC terms apply to a waveform such as this.

Notes 83

I purposely omit the velocity of light, as well as the time/distance/velocity equation, so that students will have to do some simple research this calculate this value. Neither of these concepts is beyond high-school level science students, and should pose no difficulty at all for college-level students to find on their own.

Notes 84

Students must properly interpret the oscilloscope's display, then correctly convert to RMS units, in order to obtain the correct answer for this question.

Notes 85

Many electronics students I've talked to seem to think that the RMS value of a waveform is always $\frac{\sqrt{2}}{2}$, no matter what the waveshape. Not true, as evidenced by the answer for this question!

Students must properly interpret the oscilloscope's display in order to obtain the correct answer for this question. The "conversion" to RMS units is really non-existent, but I want students to be able to explain *why* it is and not just memorize this fact.

Notes 86

This question is nothing more than an exercise in Lissajous figure interpretation.

Notes 87

Not only is the quotation funny, but it is startling as well, especially to those of us who were born without any computers in our homes at all, much less multiple personal computers.

A point I wish to make in having students research the term "microcontroller" is to see that most of the computers in existence are not of the variety one ordinarily thinks of by the label "computer." Those doorknob computers – as well as engine control computers in automobiles, kitchen appliances, cellular telephones, biomedical implants, talking birthday cards, and other small devices – are much smaller and much more specialized than the "general purpose" computers people use at their desks to write documents or surf the internet. They are the silent, unseen side of the modern "computer revolution," and in many ways are more appropriate for beginning students of digital electronics to explore than their larger, general-purpose counterparts.

Notes 88

Note that I did not bother to explain my extremely terse answer. This is a subject I desire students to think long and hard about, for the real answer(s) to this question are the reasons driving all development of programmable digital devices.

Notes 89

The purpose of this question is for students to realize that the microcontroller must be told to "loop" through the light blinking instructions. Really, this is just an illustration of loops in a practical context.

In case you're wondering why I write in pseudocode, here are a few reasons:

- No prior experience with programming required to understand pseudocode
- It never goes out of style
- Hardware independent
- No syntax errors

If I had decided to showcase code that would actually run in a microcontroller, I would be dooming the question to obsolescence. This way, I can communicate the spirit of the program without being chained to an actual programming standard. The only drawback is that students will have to translate my pseudocode to real code that will actually run on their particular MCU hardware, but that is a problem guaranteed for some regardless of which real programming language I would choose.

Of course, I could have taken the Donald Knuth approach and invented my own (imaginary) hardware and instruction set . . .

Notes 90

The purpose of this question is for students to understand what a "WHILE" loop represents in practical terms: a loop with condition(s). It also contrasts conditional looping against unconditional looping, and shows how both play a part in interactive systems such as this one.

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Notes 91

Although this logic function could have been implemented easier and cheaper in hard-wired (gate) logic, the purpose is to get students to think of performing logical operations by a sequenced set of instructions inside a programmable device (the MCU). This is a conceptual leap, basic but very important.

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Notes 97

The purpose of this question is to get students thinking in terms of "digital" quantities, which by their very nature are non-continuous. It is important to note that the concepts of continuous and discrete quantities are not limited to electronics, but are found in a variety of places in every-day life.

It should be noted that some of these determinations are subjective. The voltage output by a comparator may be considered discrete on a large time scale, but there is a measurable transition from "high" voltage to "low" voltage in which the output voltage is somewhere between full saturation limits.

Notes 98

One challenge to answering this question is for (young) students to figure out what a slide rule is!

Notes 99

While this may seem to be a very elementary question, it is important to get students to realize just what logic states are, in their physical representations. Too often I read textbooks and other digital logic tutorials that leap the student immediately into a boolean analysis of gate circuits, with everything operating off of abstract 0's and 1's (or "low's" and "high's"), without properly introducing the electrical nature of these states to students. Remember, your students should be quite familiar with electrical circuits, including analog transistor and op-amp circuits, by now, so beginning their study of gates from an electrical perspective should be natural for them. Only after they realize how logic states are represented by voltages do I recommend discussing gates and truth tables.

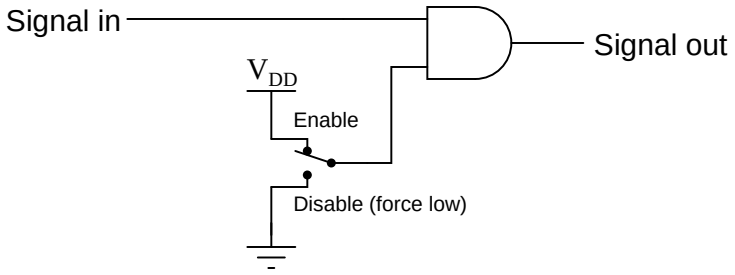
Notes 100

Diode-resistor gate circuits such as this are rarely used in real digital circuitry because they have no capacity to *amplify* weak input signals. They also have no capacity for signal inversion, rendering them incapable of representing a great many logic function types. Gates made from transistors are much preferred over diode-resistor technology.

Notes 101

This is a very useful way to think of the different logic gate types, as often you are faced with a choice of which gate type to use for a specific function in a digital circuit based on a requirement cast in these terms ("Any *blank* input guarantees a *blank* output").

For example, we might need a gate to perform a "disable" function for a digital signal:



Considered in terms of what input state forces a low output, the choice to use an AND gate becomes obvious.

Notes 102

There isn't much to comment on here, but this is a concept some students do not immediately see (how gates work with more than two inputs).

Notes 103

A helpful way for students to think about this question is to consider gates in terms of what input state *forces* the output to go to a particular state. For example, AND gate outputs are forced low by any low input, therefore the unused input had better not be tied to ground – the only remaining option is to tie it high.

Notes 104

This question is a good review of bipolar junction transistor theory.

Notes 105

This true story was told to me by one of my former students, who had some previous experience with electronics maintenance prior to enrolling in my class. The moral of this story, of course, is the sensitivity of TTL logic circuits to power supply voltage variations. This will (and should!) surprise many of your students, who are probably used to seeing the rather wide voltage limits of opamps and other analog circuitry.

Notes 106

Many students find the waveform analysis of digital circuits intimidating at first, until they understand that it is nothing more than a graphical representation of "0" and "1" logic states over time. Ask your students to share their "tips" on how to relate waveforms to truth tables, and in particular how they answered this particular question.

Just for fun, you might want to ask your students to identify where in time the toggle switch is open, and where it is closed. Some students may answer backwards to this question, if they haven't carefully considered how the toggle switch is connected in this circuit!

Notes 107

Schmitt trigger gates are indispensable for certain logic circuit applications. It is important that students recognize their function and utility.

Incidentally, this question provides a good opportunity to review magnetic hysteresis curves, since it's probably been awhile since students last studied electromagnetism theory!

Notes 108

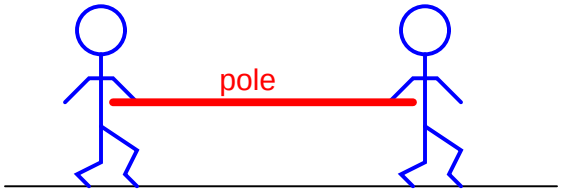
Ahhh, the vestiges of yesterday's technology! What can I say? Sometimes terms "stick" even when it makes little sense for them to.

Notes 109

This very important concept is best understood from the perspective of *conventional* current flow notation. The terms seem backward when electron flow notation is used to track current through the output transistor.

One point of confusion I've experienced among students is that current may go either direction (in or out) of a gate with totem-pole output transistors (able to sink or source current). Some students seem to have a conceptual difficulty with current going *in* to the *output* terminal of a gate circuit, because they mistakenly associate the "out" in *out*put as being a reference to direction of current, rather than direction of information or data.

An analogy I've used to help students overcome this problem is that of two people carrying a long pole:



Suppose these people are in a dark, noisy room, and they use the pole as a means of simple communication between them. For example, one person could tug on the pole to get the other person's attention. Perhaps they could even develop a simple code system for communicating thoughts (1 tug = hello ; 2 tugs = good-bye ; 3 tugs = I think this is a silly way to communicate ; 4 tugs = let's leave this room ; etc.). If one of the persons *pushes* on the pole rather than *pulls* on the pole to get the other person's attention, does the direction of the pole's motion change the direction of the communication between the two persons? Of course not. Well, then, does the direction of current through the output terminal of a gate change the direction that *information* flows between two interconnected gates? Whether a gate sources current or sinks current to a load has no bearing on the "output" designation of that gate terminal. Either way, the gate is still "telling the load what to do" by exercising control over the load current.

Notes 110

By examining one of the ancillary benefits of using CMOS instead of TTL, students get a good review of inductor and transistor theory. Ask your students to explain why a TTL gate *would* require the relay coil to have a commutating diode, lest the gate be destroyed by inductive "kickback."

Notes 111

Based on their knowledge of thyristors, your students should be able to tell you how to best "unlatch" a CMOS gate stuck in this condition. Challenge them with this problem, and also with the question of how one might detect such a condition as it's happening.

Mention to your students that not all CMOS families exhibit this problem, and that manufacturers have been keen to address serious design faults such as these. If nothing else, though, this should reinforce the lesson that one should *never* exceed the supply rail voltage for any type of active circuit, be it an op-amp, gate, or something else, unless expressly permitted by the manufacturer.

Notes 112

You may underscore this principle by stating to your students that you may walk up to a piece of conductive foam with lots of CMOS chips inserted into it, and touch it with your static-charged finger, with no damage. Even if you draw a spark between your finger and the foam (or any chip pin stuck into the foam), the chips will all be protected because they experience no voltage *between* their pins.

Notes 113

Discuss these diagrams with your students, noting any significant advantages and disadvantages of each convention.

In reference to the challenge question, the symbols "L1" and "L2" are very common designations for AC power conductors. Be sure your students have researched this and know what these labels mean!

Notes 114

Discuss with your students the sources of electrical power for both circuits here: the relay control circuit and the motor itself. Challenge your students to explore this concept by asking them the following questions:

- Are the two sources necessarily the same?
- How does the convention of linking relay coils with contacts by name (rather than by dashed lines and proximity) in ladder diagrams benefit multiple-source circuits such as this one?
- Do these circuits even have to be drawn on the same page?

Notes 115

This circuit is known as a *latching* circuit, because it "latches" in the "on" state after a momentary action. The contact in parallel with the "Run" switch is often referred to as a *seal-in contact*, because it "seals" the momentary condition of the Run switch closure after that switch is de-actuated.

The follow-up question of how we may make the motor stop running is a very important one. Spend time with your students discussing this practical design problem, and implement a solution.

Notes 116

When I first heard of a switch having "Form C" contacts, I had absolutely no idea what it meant. I was quite familiar with "single-pole, double-throw," but not this new term. Different industries often use different terms for describing the same things. Your students should be made aware that there is a tendency for people to become "isolated" within their respective industries or fields of expertise, to the point where they may be unaware of alternative terms for the same things (Form-C versus SPST is a good example of this). Your students may even find themselves misjudged by others for not knowing the peculiar and specialized terms used within certain industries, when they first obtain employment. In many ways it is akin to the misunderstandings arising when different cultures meet: people have the general tendency to think their way of doing things is the *only* way. Bridging such cultural divides requires patience, humility, and tact.

Notes 117

The ultimate purpose of this question is not to ascertain the effects of a particular fault so much as it is to derive a general rule regarding the construction of industrial control circuits. Students should be able to see the benefits of having L2 (the grounded power rail) on the right-hand side of the circuit, but can they induce the general safety principle to be applied in all control circuits? What is "special" about having L2 on the right-hand side of the ladder diagram?

Notes 118

Discuss with students the fact that relay coils and contacts need not be located near each other in ladder diagrams. While this may be confusing at times, it is a very flexible feature of ladder logic notation, because it gives the author the freedom to locate relay contacts where it makes the most visual sense in the "output" rung of the diagram, without having to coordinate locations of coil and contact as is generally necessary in traditional schematic diagrams. Instead, relay contacts are associated with their respective coils *by label*, not by proximity on the diagram.

Notes 119

This question provides a good opportunity for students to practice analyzing relay logic circuits, and it also foreshadows DeMorgan's Theorem in its dual implementation of the NOR function. Note to your students how more than one contact is being used on control relays CR1 and CR2!